Intel® 830 Chipset Platform

Design Guide

January 2005

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Revision History

Rev.	Description	Date
001	Initial Release	July 2001
002	Updates include: • Added Design Guideline clarification for 830M and 830MG chipset • Added support for Mobile Intel Celeron® Processors	October 2001
003	Updates include: • Section 5. Graphics Memory Design Guidelines removed • Added Section 6.5 for GMBUS pull-up recommendations • Added RTC material to provide for more robust and accurate RTC solutions • Minor LAN clarifications • Table 47 – ICH3-M 1.8 V Core @ S0 Max Power Consumption updated • Section 11.1.5 - Revised V5REF_Sus connection guidelines • Section 11.2.3 - 3.3 V/V5REF Sequencing clarified • Table 45 – V5REF_Sus decoupling updated • Miscellaneous revisions to Schematic and Layout Checklist	January 2002
004	Updates include: • Updated p. 45 of the schematics	November 2002
005	Updates include: • Updated p. 45 of the schematics	January 2005

1. Introduction

This design guide organizes Intel's design recommendations for Intel® 830 Chipset family systems. This document presents design recommendations and a system checklist. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues.

1.1. Related Documents

The following documents should be used as references

- *Mobile Intel® Pentium® III Processor-M Datasheet* (298340-003)*:* Contact http://developer.intel.com/design/Mobile/datashts/298340.htm
- *Mobile Intel® Celeron® Processor (0.18 µ) in Micro-FCBGA and Micro-FCPGA Packages Datasheet (298514-002): Contact* http://developer.intel.com/design/Mobile/datashts/298514.htm
- *Mobile Intel® Celeron® Processor (0.13µ) in Micro-FCBGA and Micro-FCPGA Packages Datasheet (298517-003): Contact* http://developer.intel.com/design/Mobile/datashts/298517.htm
- *Intel® 830 Chipset Family Datasheet* (298338-003)*: Contact* http://developer.intel.com/design/chipsets/datashts/298338.htm
- *Intel® I/O Controller Hub 3 (ICH3-M) Datasheet* (290716-001)*: Contact* http://developer.intel.com/design/chipsets/datashts/290716.htm
- *Intel 82801 Cam I/O Controller Hub 3 (ICH3-M) Specification Update As July 2001: Contact* http://developer.intel.com/design/chipsets/specupdt/290718.htm
- *Intel® 82807AA Video Controller Hub (VCH) Datasheet* (290690-001)*: Contact* http://developer.intel.com/design/chipsets/datashts/290690.htm
- *PCI Local bus Specification 2.2*: Contact www.pcisig.com
- *Advanced Graphic Port (AGP) 2.0 Specification*: Contact ftp://download.intel.com/technology/agp/downloads/agp20.pdf
- *Advanced Configuration and Power Management (ACPI) Specification 1.0b & 2.0*: Contact http://www.teleport.com/~acpi/
- The AC'97 2.1 Specification is on the Intel website: http://developer.intel.com/ial/scalableplatforms/audio/index.htm

1.2. System Overview

The Intel 830 Chipset family consists of two main components: 82830 (MP/M/MG) Graphics Memory Controller Hub (GMCH-M) and 82801CAM I/O Controller Hub 3 (ICH3-M). These components are interconnected via an Intel proprietary interface called Hub Interface. The Hub Interface is designed into the Intel 830 Chipset family to provide an efficient communication between components.

Additional hardware platform features include the processor interface, system memory interface (SDRAM), and an AGP interface. The 830 Chipset family is optimized for the Mobile Intel® Pentium®

III Processor-M, the Mobile Intel® Celeron® Processor (0.13 µ) in Micro-FCBGA and Micro-FCPGA Packages, and the Mobile Intel® Celeron® Processor (.18 µ) in Micro-FCBGA and Micro-FCPGA Packages (hereafter referred to as Mobile Intel Celeron Processors). This product provides flexibility and scalability in graphics subsystem performance. The Accelerated Hub Architecture interface (the chipset component interconnect) is designed into the chipset to provide an efficient, high bandwidth, communication channel between the GMCH-M and the ICH3-M. The chipset architecture also enables a security and manageability infrastructure through the Firmware Hub (FWH) component.

An ACPI compliant Intel 830 Chipset family platform can support the *Full-On (S0), Power On Suspend (POS)(S1-M), Suspend to RAM (STR)(S3), Suspend to Disk (STD) (S4), and Soft-Off (S5)* power management states. Through the use of an appropriate LAN device, the chipset also supports *wake-on LAN** for remote administration and troubleshooting. The chipset architecture removes the requirement for the ISA expansion bus that was traditionally integrated into the I/O subsystem of PCIsets/AGPsets. This removes many of the conflicts experienced when installing hardware and drivers into legacy ISA systems. The elimination of ISA provides true *plug-and-play* for the platform. Traditionally, the ISA interface was used for audio and modem devices. The addition of AC'97 allows the OEM to use *software configurable* AC'97 audio and modem coder/decoders (codecs) instead of the traditional ISA devices.

1.2.1. System Features

The Intel 830 Chipset family contains two *core* components: the GMCH-M and the ICH3-M. The GMCH-M integrates a 133 MHz, P6 family Processor System Bus (PSB) controller, AGP (1X/2X/4X) discrete graphics card interface (available only with the Intel 830M and Intel 830MP chipsets) 133-MHz SDRAM controller, and a high-speed Accelerated Hub Architecture interface for communication with the ICH3-M. The ICH3-M integrates an Ultra ATA 100/66/33 controller, USB host controller that supports USB 1.1 specification, LPC interface, FWH Flash BIOS interface controller, PCI interface controller, AC'97 digital controller and a Hub Interface for communication with the GMCH-M.

Figure 1. Basic Intel 830MP System Block Diagram

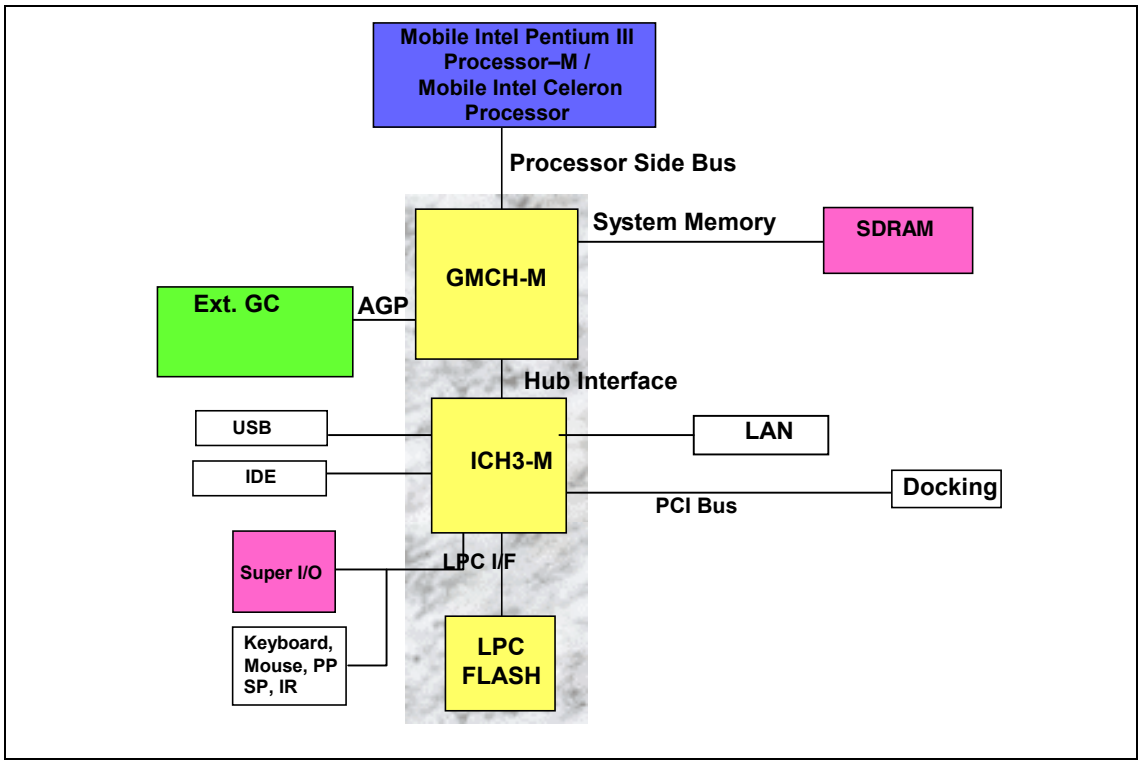


Figure 2. Basic Intel 830M System Block Diagram

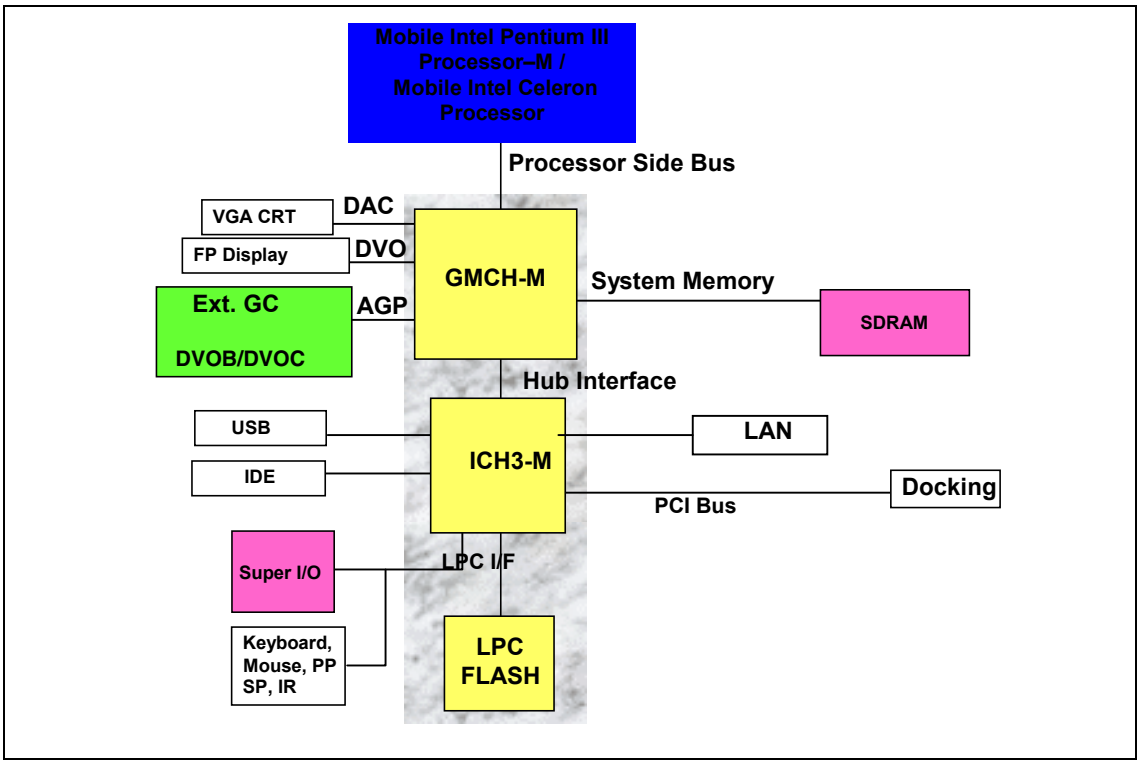
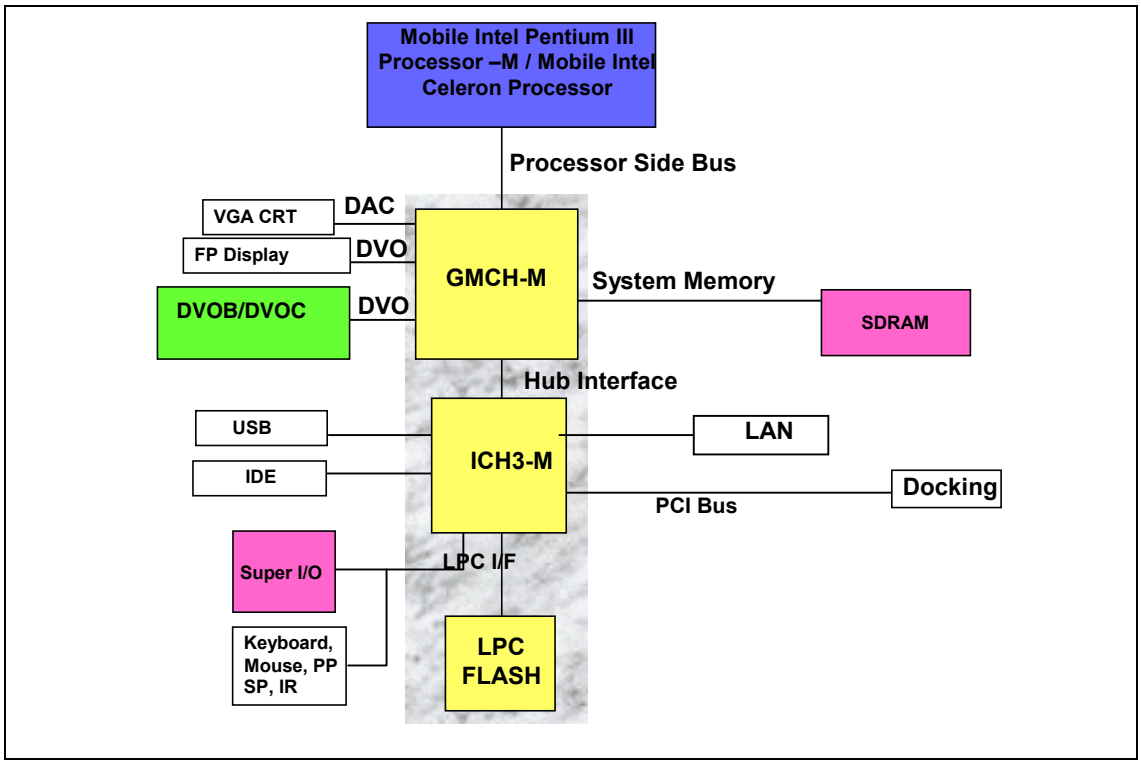


Figure 3. Basic Intel 830MG System Block Diagram



1.2.2. Intel 830MP Chipset Component Features

1.2.2.1. Intel 830MP Chipset GMCH-M

1.2.2.1.1. Processor System Bus Support

- Optimized for the Mobile Intel Pentium III Processor-M and Mobile Intel Celeron Processors at 133-MHz processor system bus frequency
- AGTL bus driver technology (gated AGTL receivers for reduced power)
- Supports 32-bit AGTL bus addressing (no support for 36-bit address extension)
- Supports Uniprocessor (UP) systems

1.2.2.1.2. Integrated System Memory DRAM Controller

- Supports up to two double-sided SO-DIMMs (four rows)
- Up to 1.0 GB using 512-Mb technology
- 133-MHz SDRAM interface
- 64-bit data interface
- Standard Synchronous DRAM (SDRAM) Support (x-1-1-1 access)
- Supports only 3.3-V SO-DIMM DRAM configurations
- No registered SO-DIMM support
- Support for Symmetrical and Asymmetrical DRAM addressing
- Support for x16 DRAM device widths
- Refresh Mechanism: CAS-before-RAS only
- Support for SO-DIMM Serial Presence Detect (SPD) scheme via SMBus interface
- STR power management support via self refresh mode using CKE

1.2.2.1.3. Accelerated Graphics Port (AGP) Interface

- Supports AGP 2.0 data transfers
- Supports a single AGP (4X/2X/1X) device (either via a connector or on the motherboard)
- AGP Vddq=1.5 V support only
- Synchronously coupled to the host with 1:2 clock ratio
- High priority access support
- Delayed transaction support for AGP reads that cannot be serviced immediately
- AGP semantic traffic to the DRAM is not snooped on the PSB and is therefore not coherent with the CPU caches

1.2.2.2. Packaging/Power

- 625 mBGA (37.5 mm * 37.5 mm)
- 1.25 V (± 5%) core and mixed 3.3 V, 1.5 V, 1.8 V, and AGTL I/O

1.2.2.3. I/O Controller Hub (ICH3-M)

ICH3-M provides the I/O subsystem with access to the rest of the system:

- Upstream Accelerated Hub Architecture interface for access to the GMCH-M
- PCI 2.2 interface (6 PCI Req/Grant Pairs)
- Bus Master IDE controller (supports Ultra ATA/100, Ultra ATA/66, Ultra ATA/33 multiword PIO modes for transfers up to 100 MBytes/sec.)
- USB 1.1 Controller
- I/O APIC
- SMBus Controller
- FWH Interface
- LPC Interface
- AC'97 2.1 interface
- Alert-On-LAN
- IRQ Controller
- Packaging/Power
- 421 mBGA (37.5 mm x 37.5 mm)
- 3.3-V and 1.8-V core; 1.80-V and 3.3-V standby

1.2.2.4. Firmware Hub (FWH)[1]

- An integrated hardware Random Number Generator (RNG)
- Register-based locking
- Hardware-based locking
- 5 GPIs

1.2.2.4.1. Packaging/Power

- 32-Pin PLCC
- 3.3-V core and 3.3 V/12 V for fast programming
  - Register-based locking

1.2.3. Intel 830M Chipset Component Features

1.2.3.1. Intel 830M Chipset GMCH-M

1.2.3.1.1. Processor System Bus Support

- Optimized for the Mobile Intel Pentium III Processor-M and Mobile Intel Celeron Processors at 133-MHz processor system bus frequency
- AGTL bus driver technology (gated AGTL receivers for reduced power)
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- AGP semantic traffic to the DRAM is not snooped on the PSB and is therefore not coherent with the CPU caches

1.2.3.1.4. Integrated Graphics Controller

- 256-bit graphics core
- Texture mapped 3D with point sampled, Bilinear, Trilinear, and Anisotropic filtering
- Hardware setup with support for strips and fans
- Hardware motion compensation assist for software MPEG/DVD decode
- Digital Video Out (DVOA/B/C) interfaces add support for digital displays and TV-out
- PC 99 and PC 2001 Compliant
- Integrated 330-MHz RAMDAC

1.2.3.2. Packaging/Power

- 625 mBGA (37.5 mm * 37.5 mm)
- 1.25 V (± 5%) core and mixed 3.3 V, 1.5 V, 1.8 V, and AGTL I/O

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- SMBus Controller
- FWH Interface
- LPC Interface
- AC'97 2.1 interface
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- 421 mBGA (37.5 mm x 37.5 mm)
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- Register-based locking
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- 5 GPIs

1.2.3.4.1. Packaging/Power

- 32-Pin PLCC
- 3.3-V core and 3.3-V/12-V for fast programming
  - Register-based locking

1.2.4. Intel 830MG Chipset Component Features

1.2.4.1. Intel 830MG Chipset GMCH-M

1.2.4.1.1. Processor System Bus Support

- Optimized for the Mobile Intel Pentium III Processor-M and Mobile Intel Celeron Processors at 133-MHz processor system bus frequency
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- Hardware-based locking
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1.2.4.4.1. Packaging/Power

- 32-Pin PLCC
- 3.3-V core and 3.3 V/12 V for fast programming
  — Register-based locking

2. General Design Considerations

This section documents motherboard layout and routing guidelines for Intel 830 Chipset family platforms. This section does not discuss the functional aspects of any bus or the layout guidelines for an add-in device.

If the guidelines listed in this document are not followed, it is very important that thorough signal integrity and timing simulations are completed for each design. Even when the guidelines are followed, critical signals should be simulated to ensure proper signal integrity and flight time. Any deviation from the guidelines should be simulated.

The trace impedance typically noted (i.e. 55 Ω ± 15%) is the "nominal" trace impedance for a 5-mil wide trace. That is, the impedance of the trace when not subjected to the fields created by changing current in neighboring traces. When calculating flight times, consider the minimum and maximum impedance of a trace, which is based on the switching of neighboring traces. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce settling time.

Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. In order to minimize the effects of trace-to-trace coupling, the routing guidelines documented in this section should be followed.

Additionally, these routing guidelines are created using a PCB *stackup*.

2.1. Nominal Board Stackup

The Intel 830 Chipset family platform requires a board stackup yielding a target impedance of 55 Ω ± 15% with a 5-mil nominal trace width for all interfaces.

3. Processor System Bus Design Guidelines

3.1. Introduction

Featuring a 133-MHz Processor System Bus with AGTL signaling, the Mobile Intel Pentium III Processor-M and Mobile Intel Celeron Processors will run at a higher core speed than previous generation IA-32 processor. The Mobile Intel Pentium III Processor-M and Mobile Intel Celeron Processors continue to be hardware and software compatible with the current Mobile Intel Pentium III Processors. The Mobile Intel Pentium III Processor-M, based on 0.13-micron technology, is available in Micro-Flip Chip Pin Grid Array (Micro-FCPGA) and Micro-Flip Chip Ball Grid Array (Micro-FCBGA) packages. The Mobile Intel Celeron Processor, based on both 0.13-micron and 0.18-micron technology, is available in Micro-FCBGA and Micro-FCPGA Packages.

The following layout guidelines support designs using the Mobile Intel Pentium III Processor-M/the Mobile Intel Celeron Processors and the Intel 830 Chipset family. Due to on-die Rtt resistors on both the processor and the chipset, additional resistors do not need to be placed on the motherboard for most PSB signals. The lone exception is on the CPURST# signal which requires a 56 Ω pull-up to Vtt on the processor end of the transmission line.

3.2. Processor System Bus (PSB) Routing Guidelines

3.2.1. Initial Timing Analysis

The following table lists the AGTL component timings of the processors and the Intel 830 Chipset family GMCH-M defined at the pins. For more detail, please also consult *Intel® 830 Chipset Family Datasheet*.

Table 1. Processor and Chipset AGTL Parameters for Example Calculations

IC Parameters	Mobile Intel Pentium III Processor-M (133-MHz System Bus)	GMCH-M	Notes
Clock to Output maximum (T_{CO_MAX})	3.25 ns	4.1 ns	1
Clock to Output minimum (T_{CO_MIN})	0.40 ns	1.05 ns	1
Setup time (T_{SU_MIN})	0.95 ns	2.65 ns	1,2
Hold time (T_{HOLD})	1.0 ns	0.10 ns	

NOTES:

1. *Numbers in table are for reference only*. These timing parameters are subject to change. Check the appropriate component documentation for the valid timing parameter values.
2. T_{SU_MIN} = 2.65 ns assumes that the Intel 830 Chipset family GMCH-M sees a minimum edge rate equal to 0.3 V/ns.

The following table gives an example of AGTL initial maximum flight time and Table 3 is an example minimum flight time calculation for a 133-MHz, uniprocessor system using a Mobile Intel Pentium III Processor-M / a Mobile Intel Celeron Processor with Intel 830 Chipset family system bus.

Note: Assumed values for clock skew and clock jitter were used.

Clock skew and clock jitter values are dependent on the clock components and distribution method chosen for a particular design and must be budgeted into the initial timing equations as appropriate for each design.

Table 2 and Table 3 are derived using the following timing components:

- CLK_{SKEW} = The maximum allowable skew between the 133-MHz clocks driven by the clock chip to the processor and GMCH-M. Assumed to be 150 ps.
- CLK_{JITTER} = The maximum allowable short-term variation in the clock edge from its ideal position. Assumed to be 200 ps.
- T_{P-P} = Pin to pin skew due to loading effects. Assumed to be 150 ps.
- M_{ADJ} = Guardband factor. Assumed to be 100 ps

See the respective processor datasheet and appropriate Intel 830 Chipset family documentation for details on clock skew and jitter specifications. Exact details of host clock routing topology are provided with the platform design guideline.

Table 2. Example TFLT_MAX Calculations for 133-MHz Bus

Driver	Receiver	TCYC	TCO_MAX	TSU_MIN	CLKSKEW	CLKJITTER	T P-P	MADJ	Recommended TFLT_MAX
Processor	GMCH-M	7.50	3.25 ns	2.65 ns	0.15 ns	0.20 ns	0.15 ns	0.1 ns	1.00 ns
GMCH-M	Processor	7.50	4.10 ns	0.95 ns	0.15 ns	0.20 ns	0.15 ns	0.1 ns	1.85 ns

NOTE: $T_{FLT\_MAX} = T_{CYC} - T_{CO\_MAX} - T_{SU\_MIN} - Clk_{SKEW} - Clk_{JITTER} - T_{P-P} - M_{ADJ}$.

Table 3. Example TFLT_MIN Calculations (Frequency Independent)

Driver	Receiver	T_{HOLD}	T_{CO_MIN}	T_{P-P}	CLK_{SKEW}	M_{ADJ}	Recommended T_{FLT_MIN}
Processor	GMCH-M	0.10	0.40 ns	0.15 ns	0.15 ns	0.1 ns	0.10 ns
GMCH-M	Processor	1.00	1.05 ns	0.15 ns	0.15 ns	0.1 ns	0.35 ns

NOTE: $T_{FLT\_MIN} = T_{HOLD} - T_{CO\_MIN} + +CLK_{SKEW} + TP_{-P} + M_{ADJ}$.

The flight times in the previous tables include margin to account for the phenomena listed below that Intel has observed when multiple bits are switching simultaneously. These multi-bit effects can adversely affect flight time and signal quality and are sometimes not accounted for in simulation. Accordingly, maximum flight times depend on the baseboard design and additional adjustment factors or margins are recommended.

- SSO push-out or pull-in
- Rising or falling edge rate degradation at the receiver caused by inductance in the current return path, requiring extrapolation that causes additional delay.
- Crosstalk on the PCB and internal to the package can cause variation in the signals.

There are additional effects that **may not** necessarily be covered by the multi-bit adjustment factor and should be budgeted as appropriate to the baseboard design. Examples include:

- The effective board propagation constant (S_{EFF}), which is a function of:
  - Dielectric constant (ε_r) of the PCB material.
  - The type of traces connecting the components (stripline or microstrip).
  - The length of the trace and the load of the components on the trace. Note that the board propagation constant multiplied by the trace length is a **component** of the flight time **but not necessarily equal to** the flight time.

3.3. General Topology and Layout Guidelines

The following topology and layout guidelines are for the processor interface to the Intel 830 Chipset family GMCH-M.

Table 4. Processor System Bus Data Signal Routing Guidelines

Signal Names		Topology	Total Trace Length		Nominal Impedance (ohms)	Width and Spacing (mils)
CPU	GMCH-M		Max (inches)	Min (inches)		
D[63:0]#	HD[63:0]#	TOP 1	4.0	2.0	55 ± 15%	5 & 10

Table 5. Processor System Bus Address Signal Routing Guidelines

Signal Names		Topology	Total Trace Length		Nominal Impedance (ohms)	Width and Spacing (mils)
CPU	GMCH-M		Max (inches)	Min (inches)		
A[31:3]#	HA[31:3]#	TOP 1	4.0	2.0	55 ± 15%	5 & 10

Table 6. Processor System Bus Control Signal Routing Guidelines

Signal Names		Topology	Total Trace Length		Nominal Impedance (ohms)	Width and Spacing (mils)
CPU	GMCH-M		Max (inches)	Min (inches)		
RESET#	CPURST#	TOP 2	4.0	2.0	55 ± 15%	5 & 10
BNR#	BNR#	TOP 1	4.0	2.0	55 ± 15%	5 & 10
REQ[4:0]#	HREQ[4:0]#	TOP 1	4.0	2.0	55 ± 15%	5 & 10
BPRI#	BPRI#	TOP 1	4.0	2.0	55 ± 15%	5 & 10
DEFER#	DEFER#	TOP 1	4.0	2.0	55 ± 15%	5 & 10
LOCK#	HLOCK#	TOP 1	4.0	2.0	55 ± 15%	5 & 10
TRDY#	HTRDY#	TOP 1	4.0	2.0	55 ± 15%	5 & 10
DRDY#	DRDY#	TOP 1	4.0	2.0	55 ± 15%	5 & 10
ADS#	ADS#	TOP 1	4.0	2.0	55 ± 15%	5 & 10
DBSY#	DBSY#	TOP 1	4.0	2.0	55 ± 15%	5 & 10
HIT#	HIT#	TOP 1	4.0	2.0	55 ± 15%	5 & 10
HITM#	HITM#	TOP 1	4.0	2.0	55 ± 15%	5 & 10
RS[2:0]#	RS[2:0]#	TOP 1	4.0	2.0	55 ± 15%	5 & 10

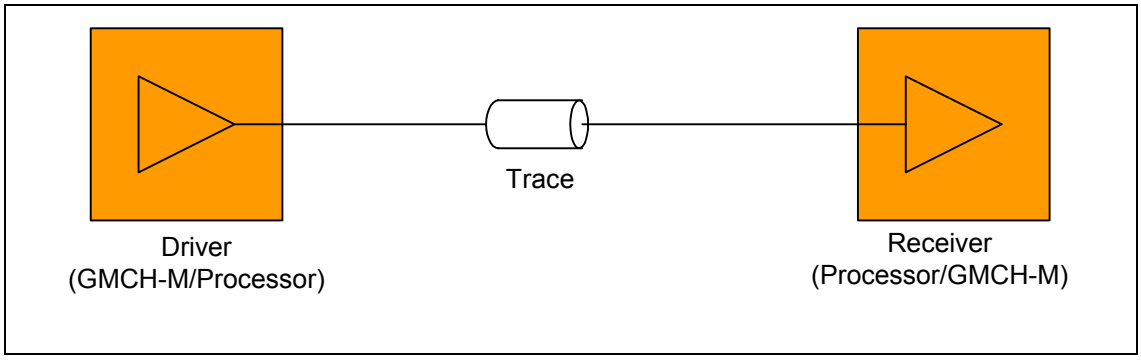
NOTE: Trace width of 5 mils and trace spacing of 10 mils within signal groups. Spacing between signal groups (address, data and control) should be 25 mils and for spacing from other (3.3 V) signals should be 25 mils.

3.3.1. Topologies

3.3.1.1. Topology 1

Topology 1 requires that the signals be routed directly from the CPU to the chipset. Both the CPU and the chipset have on-die termination; which removes the need for termination resistors on the motherboard. Thus, the signals are dual-end terminated.

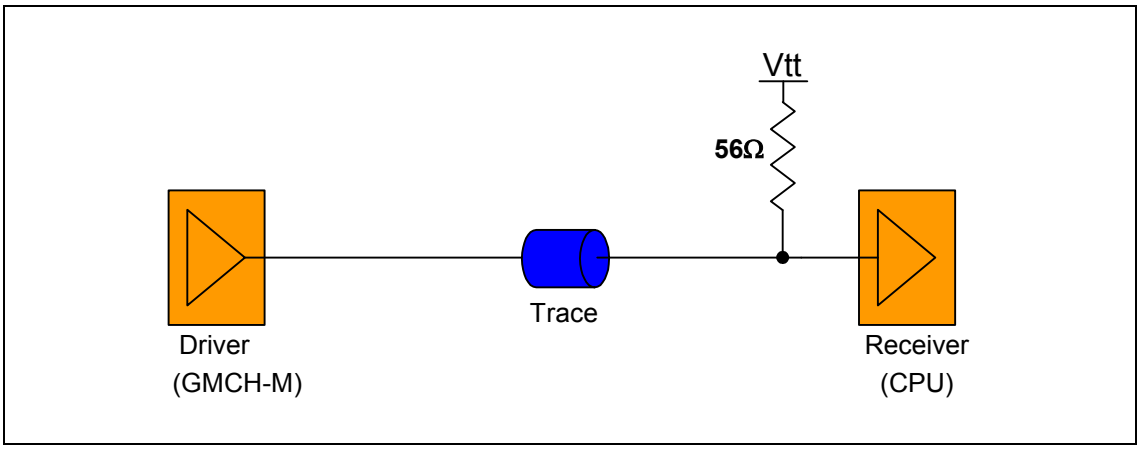
Figure 4. PSB Routing Topology 1



3.3.1.2. Topology 2

Topology 2 applies to only one signal; processor pin name Reset# and chipset ball name CPURST#. Topology 2 requires that there be a 56 Ω pull-up to Vtt on the trace.

Figure 5. PSB Routing Topology 2



3.3.2. Trace Routing

Trace routing requires that the traces be routed in the inner layers (1.25-V power referenced) and via down to the bottom inner layer (within 500 mils) where they will be referenced to ground. There needs to be a capacitor near the via as there is a requirement of one capacitor for every three vias. Capacitor requirements are as follows: C=100 nF, ESR=80 mΩ, ESL=0.6 nH.

3.3.3. Motherboard Layout Rules for AGTL Signals

3.3.3.1. Ground Reference

Intel recommends that AGTL signals be routed on the signal layer next to the ground layer (referenced to ground). It is important to provide effective signal return path with low inductance. The best signal routing is directly adjacent to a solid GND plane with no splits or cuts. Eliminate parallel traces between layers not separated by a power or ground plane.

3.3.3.2. Reference Plane Splits

Splits in reference planes disrupt signal return paths and increase overshoot/undershoot due to significantly increased inductance.

3.3.3.3. CPU Connector Breakout

Intel does not recommend that AGTL signals traverse multiple signal layers. Intel does recommend breaking out all signals from the connector on the same layer. If routing is tight, breakout from the connector on the opposite routing layer over a ground reference and cross over to main signal layer near the CPU connector.

Note: Following the above layout rules are critical for AGTL signal integrity, particularly for the 0.13-micron process technology.

3.3.3.4. Minimizing Crosstalk

The following general rules will minimize the impact of crosstalk in the high-speed AGTL bus design:

1. Maximize the space between traces. Maintain a minimum of 10 mils (assuming a 5-mil trace) between trace edges wherever possible. It may be necessary to use tighter spacing when routing between component pins. When traces have to be close and parallel to each other, minimize the distance that they are close together and maximize the distance between the sections when the spacing restrictions relaxes.
2. Avoid parallelism between signals on adjacent layers if there is no AC reference plane between them. As a rule of thumb, route adjacent layers orthogonally.
3. Since AGTL is a low signal swing technology, it is important to isolate AGTL signals from other signals by at least 25 mils. This will avoid coupling from signals that have larger voltage swings, such as 3.3-V system memory.
4. Select a board stack-up that minimizes the coupling between adjacent signals. Minimize the nominal characteristic impedance within the AGTL specification. This can be done by minimizing the height of the trace from its reference plane, which minimizes the crosstalk.
5. Route AGTL address, data, and control signals in separate groups to minimize crosstalk between groups. Keep at least 25 mils between each group of signals.
6. Minimize the dielectric used in the system. This makes the traces closer to their reference plane and thus reduces the crosstalk magnitude.
7. Minimize the dielectric process variation used in the PCB fabrication.
8. Minimize the cross sectional area of the traces. This can be done by narrower traces and/or by using thinner copper, but the tradeoff for this smaller cross sectional area is a higher trace resistivity that can reduce the falling edge noise margin because of the I*R loss along the trace.

3.3.4. Motherboard Layout Rules for Non-AGTL (CMOS) Signals

For all Non-AGTL (CMOS) signals, routing can be done on any layer or combination of layers.

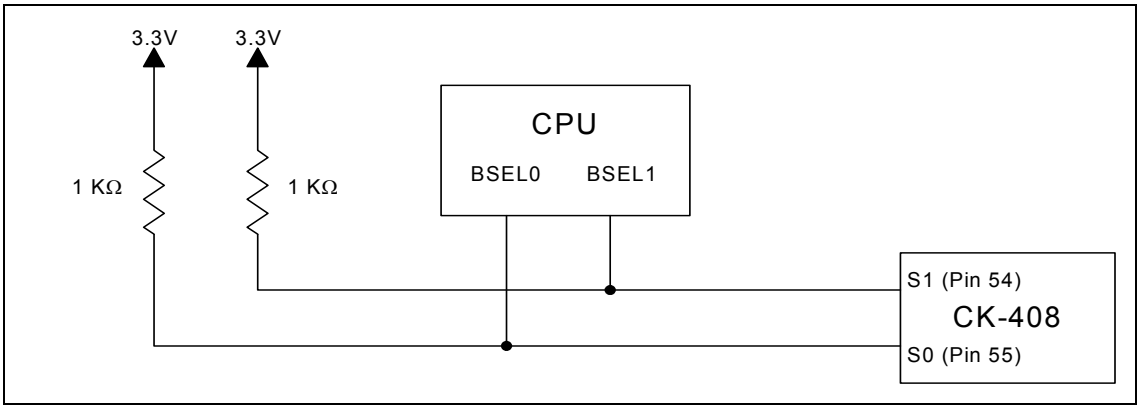
Table 7. Routing Guidelines for Non-AGTL Signals

Signal	Trace Width	Spacing to Other Traces	Trace Length
A20M#	5 mils	10 mils	1” to 8”
FERR#	5 mils	10 mils	1” to 8”
FLUSH#	5 mils	10 mils	1” to 8”
IERR#	5 mils	10 mils	1” to 8”
IGNNE#	5 mils	10 mils	1” to 8”
INIT#	5 mils	10 mils	1” to 8”
LINT[0] (INTR)	5 mils	10 mils	1” to 8”
LINT[1] (NMI)	5 mils	10 mils	1” to 8”
PICD[1:0]	5 mils	10 mils	1” to 8”
PREQ#	5 mils	10 mils	1” to 8”
PWRGOOD	5 mils	10 mils	1” to 8”
SLP#	5 mils	10 mils	1” to 8”
SMI#	5 mils	10 mils	1” to 8”
STPCLK	5 mils	10 mils	1” to 8”

3.4. BSEL[1:0] Implementation

These signals are used to select the system bus frequency. All system bus agents must operate at the same frequency. Both the Mobile Intel Pentium III Processor-M/ Mobile Intel Celeron Processors and the Intel 830 Chipset family GMCH-M operate at 133-MHz system bus frequency. Thus, BSEL[1:0] must both be pulled-up to 3.3 V through 1-kΩ resistors.

Figure 6. BSEL[1:0] Circuit Implementation



3.5. Undershoot/Overshoot Requirements

Overshoot (or undershoot) is the absolute value of the maximum voltage above the nominal high voltage or below VSS. The overshoot guideline limits transitions beyond VCC or VSS due to the fast signal edge rates. The processor can be damaged by repeated overshoot events on buffers if the charge is large enough (i.e. if the overshoot is great enough). Determining the impact of an overshoot/undershoot condition requires knowledge of the magnitude, the pulse direction and the activity factor (AF). Permanent damage to the processor is the likely result of excessive overshoot/undershoot. Violating the overshoot/undershoot guideline will also make satisfying the ringback specification difficult.

When performing simulations to determine impact of overshoot and overshoot, ESD diodes must be properly characterized. ESD protection diodes do not act as voltage clamps and will not provide overshoot or undershoot protection. ESD diodes modeled within Intel I/O Buffer models do not clamp undershoot or overshoot and will yield correct simulation results. If other I/O buffer models are being used to characterize the Mobile Intel Pentium III Processor-M /Mobile Intel Celeron Processors performance, care must be taken to ensure that ESD models do not clamp extreme voltage levels. Intel I/O buffer models also contain I/O capacitance characterization. Therefore, removing the ESD diodes from an I/O buffer model will impact results and may yield excessive overshoot/undershoot.

Refer to the respective Mobile Intel Pentium III Processor-M, Mobile Intel Celeron Processor (0.13 µ) and Mobile Intel Celeron Processor (0.18 µ) datasheets for detailed undershoot/overshoot requirements.

3.6. Processor PLL Filter Recommendations

The Mobile Intel Pentium III Processor-M/Mobile Intel Celeron Processors have internal phase lock loop (PLL) clock generators, which are analog and require a quiet power supply to minimize jitter. Please refer to the respective Mobile Intel Pentium III Processor-M, Mobile Intel Celeron Processor (0.13 µ) and Mobile Intel Celeron Processor (0.18 µ) datasheets

3.7. CPU Decoupling Guidelines for Flexible Micro-FCPGA and Micro-FCBGA Designs

Please refer to the latest *Intel® 830 Chipset Family Datasheet* and the respective Mobile Intel Pentium III Processor-M, Mobile Intel Celeron Processor (0.13 µ) and Mobile Intel Celeron Processor (0.18 µ) datasheets.

3.7.1. Vref Decoupling Design

Four 0.1-µF high frequency capacitors in a 0603 package placed near the Vref pins (within 500 mils).

3.7.2. Vcc_{CORE} Decoupling Design

Place *Twenty-Four* 0.47-µF 0603 capacitors directly under the package on the solder side of the motherboard using at least one via per capacitor node. *Ten* 10-µF X7, 6.3-V 1206-size ceramic capacitors should be placed around the package periphery near the balls. Trace lengths to the vias should be designed to minimize inductance. Avoid bending traces to minimize ESL.

All capacitors should be placed within the Micro-FCPGA and Micro-FCBGA socket cavity and mounted on the primary side of the motherboard. The capacitors are arranged to minimize the overall inductance between V_{CCP} / Vss power pins.

3.7.3. Vtt Decoupling Design

Place *Ten* 1-µF X7R 0603 ceramic capacitors close to the package. Via and trace guidelines are the same as above.

3.8. Thermal Considerations

Refer to the respective Mobile Intel Pentium III Processor-M, Mobile Intel Celeron Processor (0.13 µ) and Mobile Intel Celeron Processor (0.18 µ) datasheets for all platform thermal considerations.

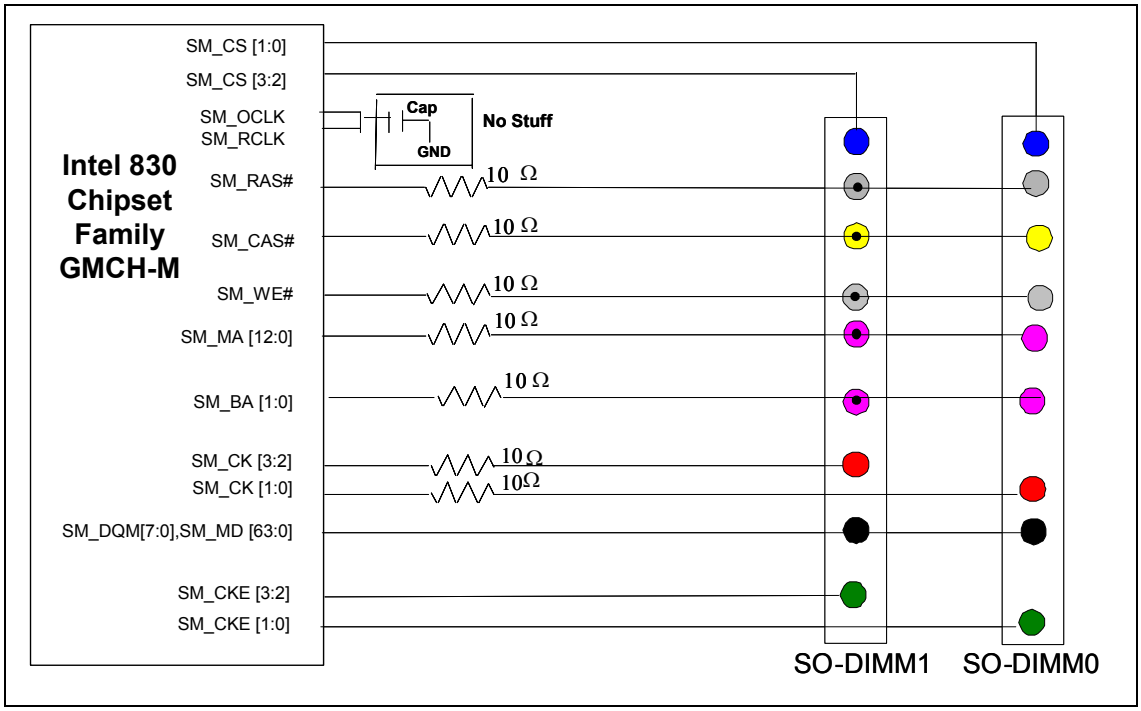
4. System Memory Design Guidelines

This section lists guidelines for routing the signal traces of the board design. The order of which signals are routed first and last will vary as some designers prefer routing all of the clock signals first, while others prefer routing all of the high-speed bus signals first. Either order can be used, as long as the guidelines listed below are followed. Intel recommends simulating the signals for proper signal integrity, flight time, and crosstalk.

4.1. System Memory Two SO-DIMM Layout Guidelines

The figures and tables below show the topology for a two SO-DIMM design and provide the minimum and maximum trace lengths to the SO-DIMM connector pads for each signal group.

Figure 7. System Memory Two SO-DIMM Block Diagram



4.1.1. Signals: SM_MA[12:0], SM_RAS#, SM_CAS#, SM_WE#, SM_BA[1:0]

Figure 8. Layout Topology for SM_MA[12:0], SM_RAS#, SM_CAS#, SM_WE#, SM_BA[1:0]

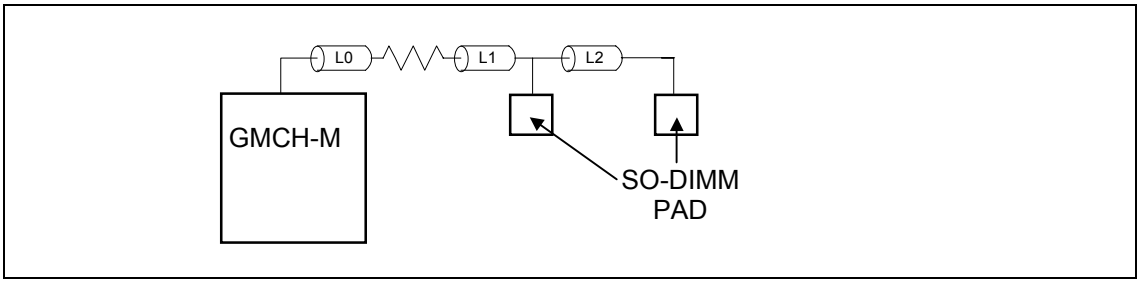


Table 8. Routing Guidelines for SM_MA[12:0], SM_RAS#, SM_CAS#, SM_WE#, SM_BA[1:0]

Section	Minimum	Maximum
L0 + L1	1.5 in	N/A
L0 + L1 + L2	N/A	6.0 in
Series R	N/A	10 Ω

4.1.2. Signals: SM_MD[63:0], SM_DQM[7:0]

Figure 9. Layout Topology for SM_MD[63:0], SM_DQM[7:0]

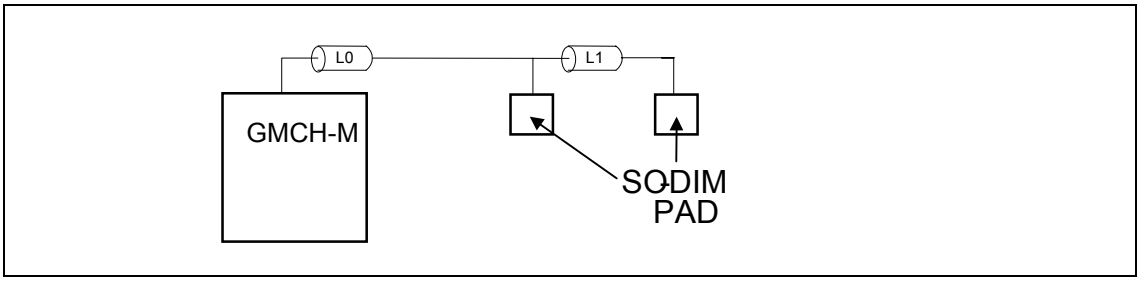


Table 9. Routing Guidelines for SM_MD[63:0], SM_DQM[7:0]

Section	Minimum	Maximum
L0 + L1	1.5 in	4.0 in
L1	N/A	0.7 in

4.1.3. Signals: SM_CS[3:0], SM_CKE[3:0]

Figure 10. Layout Topology for SM_CS[3:0], SM_CKE[3:0]

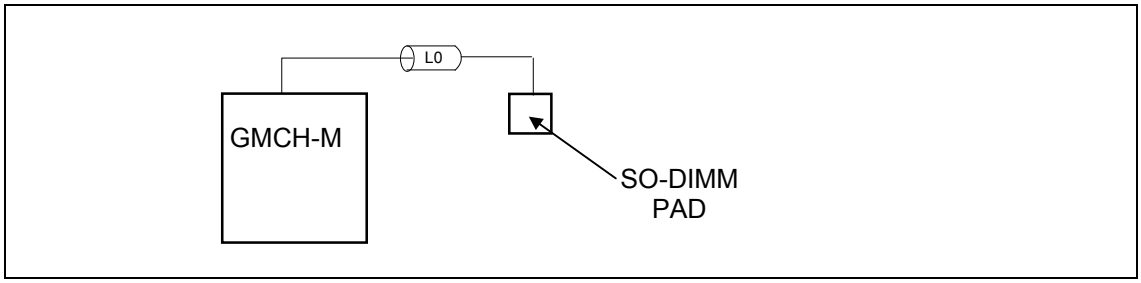


Table 10. Routing Guidelines for SM_CS[3:0], SM_CKE[3:0]

Section	Minimum	Maximum
L0	1.5 in	5.0 in

4.1.4. Signals: SM_CLK[3:0]

Figure 11. Layout Topology for SM_CLK[3:0]

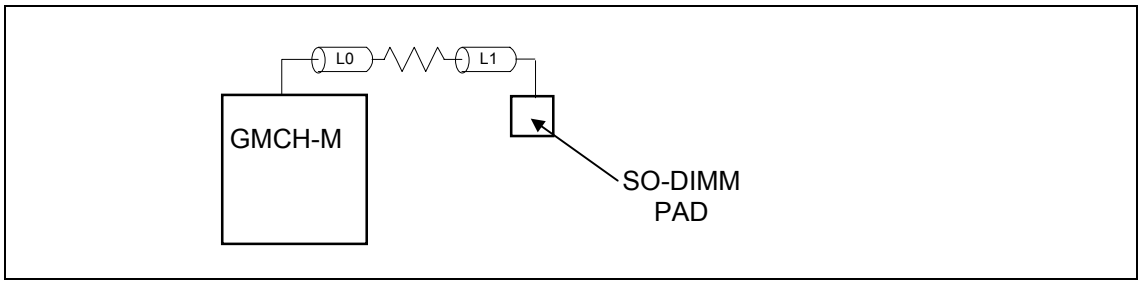


Table 11. Routing Guidelines for SM_CK[3:0]

Section	Minimum	Maximum
Series R	N/A	10 Ω
L0 + L1	4.9 in	5.1 in

4.1.5. Signal: SM_OCLK to SM_RCLK

Figure 12. Layout Topology for SM_CK[3:0]

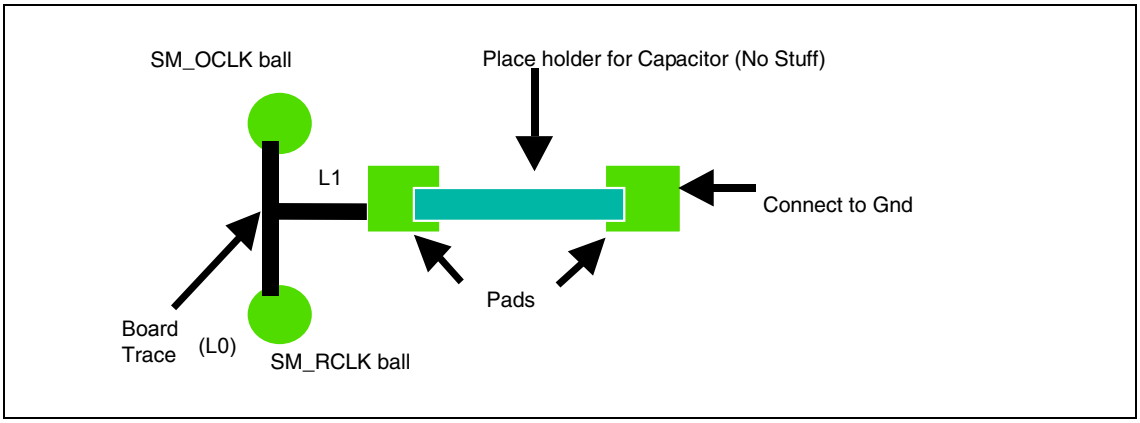


Table 12. Routing Guidelines for SM_OCLK to SM_RCLK

Section	Minimum	Maximum
L0	0.1 in	0.2 in
L1	N/A	N/A

NOTE: Trace stub to capacitor pad should be as short as possible and routed as close to the SM_RCLK ball as possible.

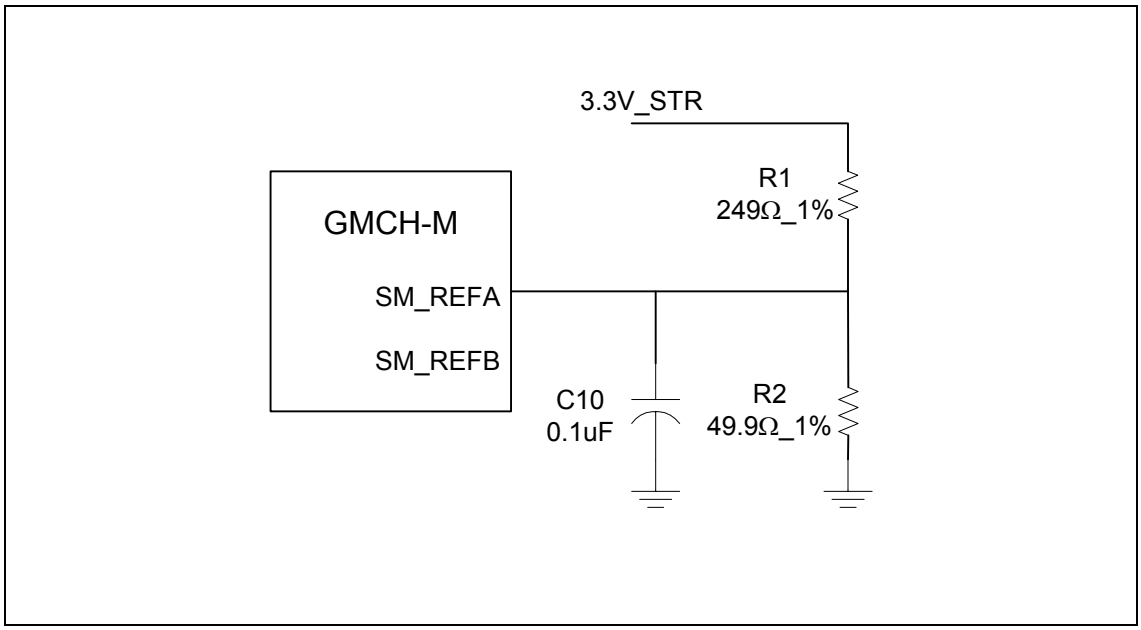
4.2. Memory Layout Recommendations

Read path sets a topology constraint due to signal integrity issues and thus creating a timing problem. Topology requires that the pads of each of the SO-DIMMS be no further than 0.70 inches from each other. Intel recommends that address and control signals have a series termination of 10 Ohms. Data lines must be swizzled for best “straight line” routing. All traces should be routed internally.

4.3. System Memory Reference Voltage

The system memory reference voltage (SM_REF) must be generated as shown below. The SM_REF should be generated from a typical resistor divider using 1% tolerance resistors. Additional decoupling is needed for the Intel 830 Chipset family GMCH-M SMSREF. Place a 0.1-µF low ESR/ESL capacitor close to the Intel 830 Chipset family GMCH-M.

Figure 13. SM_REF Implementation

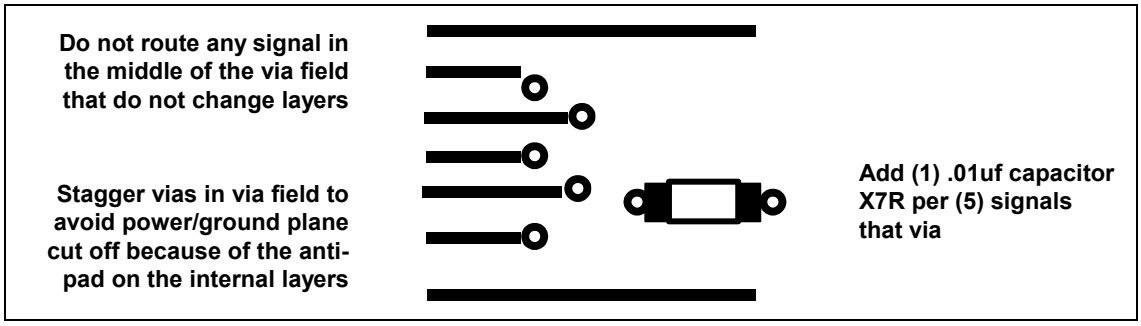


4.4. Ground Referencing

If ground referencing is not possible, the system memory signals should be single plane referenced. The order of precedence for ground referencing is SM_CLK, SM_MD, SM_DQM, SM_MA then SM_RAS#/CAS#/WE#. If single plane referencing is not possible, stitching capacitors should be added no more than 200 mils from the signal via field. Signals in the back rows of the GMCH-M ball field do not need stitching capacitors as long as the trace underneath the BGA is less than 200 mils. The stitching capacitor should be between the 3.3-V standby voltage and ground. Use one 0.01 µF, X7R capacitor per every five system memory signals that switch plane references. No more than two vias are allowed on any system memory signal.

If a group of system memory signals needs to change layer, a via field should be created and decoupling capacitor should be added at the end of the via field. Do not route signals in the middle of a via field, this will cause noise to be generated on the current return path of these signals and can lead to issues on these signals. See diagram below. The traces shown are on layer 1 only. The diagram shows the signals are changing layer and two signals that are not changing layer. Note the two signals around the via field create a keep out zone where signals that do not change layer should not be routed.

Figure 14. Plane Transition Capacitor Placement Methodology



4.5. System Memory Decoupling Guidelines

A minimum of thirteen 0.1-µF low-ESL ceramic capacitors (e.g., 0603 body type, X7R dielectric) is required and must be as close as possible to the Intel 830 Chipset family GMCH-M. They should be placed within at most 90 mils to the edge of the GMCH-M package edge for 3.3-V standby voltage decoupling, and they should be evenly distributed around the system memory interface signal field including the sides of the Intel 830 Chipset family GMCH-M where the system memory interface meets the host interface and Hub Interface.

Two topside 0.1-µF decoupling caps should be placed directly to solder balls A8 and A12, with shortest and widest VCC trace possible. Place an additional two 0.1-µF decoupling caps close to the SM_VREF[1:0] pins. There are power and GND balls throughout the system memory ball field of the GMCH-M that need good local decoupling. Make sure to use at least 14-mil drilled vias and wide traces from the pads of the capacitor to the power or ground plane to create a low inductance path. If possible, multiple vias per capacitor pad are recommended to further reduce inductance.

In order to add the decoupling capacitors within 90 mils of the GMCH-M and/or close to the vias, the trace spacing may be reduced as the traces go around each capacitor. The narrowing of space between traces should be minimal and for as short a distance as possible (500 mils max).

To further decouple the GMCH-M and provide a solid current return path for the system memory interface signals, Intel recommends that a parallel plate capacitor be added under the GMCH-M. Add a topside or bottom side copper flood under center of the GMCH-M to create a parallel plate capacitor between the 3.3-V standby voltage and GND.

4.6. Compensation

A system memory compensation resistor, SM_RCOMP is used by the Intel 830 Chipset family GMCH-M to adjust buffer characteristics to specific board and operation environment characteristics. Refer to the *Intel® 830 Chipset Family Datasheet* for details on compensation. Tie the SM_RCOMP pin of the GMCH-M to a 27.5 Ω 1% pull-down resistor to ground. Keep this trace as short as possible.

5. Intel 830MP and 830M Chipset AGP Design Guidelines

For detailed AGP interface functionality (e.g., protocols, rules, signaling mechanisms), refer to the latest *AGP Interface Specification, Revision 2.0*, which can be obtained from http://www.agpforum.org/. This design guide focuses only on specific Intel 830MP/830M Chipset platform recommendations.

5.1. AGP Interface

The *AGP Interface Specification Revision 2.0* enhances the functionality of the original AGP Interface Specification (revision 1.0) by allowing 4X data transfers (4 data samples per clock) and 1.5-V operation. In addition to these major enhancements, additional performance enhancement and clarifications, such as *fast write* capability, are included in the *AGP Interface Specification Revision 2.0*. The Intel 830MP/830M Chipset supports all of the above features in compliance with the *AGP Interface Specification Revision 2.0.*

The 4X operation of the AGP interface provides for "quad-sampling" of the AGP AD (Address/Data) and SBA (Side-band Addressing) buses. That is, the data is sampled four times during each 66-MHz AGP clock. This means that each data cycle is ¼ of 15 ns (66-MHz clock) or 3.75 ns. It is important to realize that 3.75 ns is the data cycle time; not the clock cycle time. During 2X operation, the data is sampled twice during a 66-MHz clock cycle; therefore, the data cycle time is 7.5 ns.

In order to allow for these high-speed data transfers, the 2X mode of AGP operation uses source synchronous data strobing. During 4X operation, the AGP interface recommends differential source synchronous strobing.

With data cycle times as small as 3.75 ns and setup/hold times of 1 ns, propagation delay mismatch is critical. In addition to reducing propagation delay mismatch, it is important to minimize noise. Noise on the data lines will cause the settling time to be large. If the mismatch between a data line and the associated strobe is too great or there is noise on the interface, incorrect data will be sampled.

The low-voltage operation on AGP (1.5 V) requires even more noise immunity. For example, during 1.5-V operation, V_{ilmax} is 570 mV. Without proper isolation, crosstalk could create signal integrity issues.

LOCK# and SERR#/PERR# are not supported. The AGP buffers operate in only **one** mode:

- Intel 830MP/830M AGP I/O requires 1.5-V and is not 3.3-V safe. This mode is compliant with the AGP 2.0 spec.
- AGP 4X, 2X and 1X must operate at 1.5 V. The AGP interface supports up to 4X AGP signaling. AGP semantic cycles to DRAM are not snooped on the host bus.

The Intel 830MP/830M Chipset family GMCH-M supports PIPE# or SBA[7:0] AGP address mechanisms, but not both simultaneously. Either the PIPE# or the SBA[7:0] mechanism must be selected during system initialization.

The AGP interface is clocked from the 66-MHz clock. The AGP interface is synchronous to the host and system memory interfaces with a clock ratio of 1:2 (66 MHz: 133 MHz) and to the Hub Interface with a clock ratio of 1:1 (66 MHz: 66 MHz).

5.2. AGP 2.0

The *AGP Interface Specification*, *Revision 2.0* enhances the functionality of the original *AGP Interface Specification Revision 1.0* by allowing 4X data transfers (i.e., 4 data samples per clock) and 1.5-V operation. The 4X operation of the AGP interface provides for "quad-pumping" of the AGP AD (address/data) and SBA (side-band addressing) buses. That is, data is sampled four times during each 66-MHz AGP clock. This means that each data cycle is ¼ of a 15-ns (66-MHz) clock or 3.75 ns. Note that 3.75 ns is the data cycle time, not the clock cycle time. During 2X operation, data is sampled twice during a 66-MHz clock cycle; therefore, the data cycle time is 7.5 ns. In order to allow for these high-speed data transfers, the 2X mode of AGP operation uses source-synchronous data strobing. During 4X operation, the AGP interface recommends differential source-synchronous strobing.

With data cycle times as small as 3.75 ns and setup/hold times of 1 ns, propagation delay mismatch is critical. In addition to reducing propagation delay mismatch, it is important to minimize noise. Noise on the data lines will cause the settling time to be long. If the mismatch between a data line and the associated strobe is too great or if there is noise on the interface, incorrect data will be sampled. The low-voltage operation on AGP (1.5 V) requires even more noise immunity.

5.2.1. AGP Interface Signal Groups

The signals on the AGP interface are broken into three groups: 1X timing domain signals, 2X/4X timing domain signals, and miscellaneous signals. Each group has different routing requirements. In addition, within the 2X/4X timing domain signals, there are three sets of signals. All signals in the 2X/4X timing domain must meet minimum and maximum trace length requirements as well as trace width and spacing requirements.

The signal groups are documented in the following table.

Table 13. AGP 2.0 Signal Groups

1X timing domain	RBF# WBF# ST[2:0] PIPE# REQ# GNT# PAR FRAME# IRDY# TRDY# STOP# DEVSEL#
2X / 4X timing domain	Set #1 AD[15:0] C/BE[1:0]# AD_STB0 AD_STB0#[1] Set #2 AD[31:16] C/BE[3:2]# AD_STB1 AD_STB1#[1] Set #3 SBA[7:0] SB_STB SB_STB#[1]
Miscellaneous, async	USB+ USB- OVRCNT# PME# TYPDET# PERR# SERR# INTA# INTB#

NOTE: These signals are used in 4X AGP mode ONLY.

Table 14. AGP 2.0 Data/Strobe Associations

Data	Associated Strobe in 1X	Associated Strobe in 2X	Associated Strobes in 4X
AD[15:0] and C/BE[1:0]#	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	AD_STB0	AD_STB0, AD_STB0#
AD[31:16] and C/BE[3:2]#	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	AD_STB1	AD_STB1, AD_STB1#
SBA[7:0]	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	SB_STB	SB_STB, SB_STB#

Throughout this section, the term data refers to AD[31:0], C/BE[3:0]#, and SBA[7:0]. The term strobe refers to AD_STB[1:0], AD_STB#[1:0], SB_STB, and SB_STB#. When the term data is used, it refers to one of the three sets of data signals, as in Table 13. When the term strobe is used, it refers to one of the strobes as it relates to the data in its associated group.

The routing guidelines for each group of signals (1X timing domain signals, 2X/4X timing domain signals, and miscellaneous signals) will be addressed separately.

5.2.2. AGP Busy/Stop Protocol With External Graphics Revision

The AGP_BUSY# and STP_AGP# signals allow power management signaling between an external AGP graphics controller and the ICH3-M. AGP_BUSY# indicates that the AGP device is busy. C3_STAT# (STP_AGP#) is the signal, which used for indicating to the AGP device that a C3 state transition is beginning or ending. AGP_BUSY# (ICH3-M signal) and STP_AGP# (AGP graphics controller signal) are not directly connected to the Intel 830MP and 830M Chipset GMCH-M AGPBUSY# (internal graphics controller signal) signal. For proper implementations, please consult Intel Field Application Engineers.

5.3. AGP Routing Guidelines

5.3.1. 1X Timing Domain Routing Guidelines

5.3.1.1. Trace Length Requirements for the AGP 1X

This section contains information on the 1X Timing Domain Routing Guidelines. The AGP 1X timing domain signals (refer to Table 13) have a maximum trace length of 6.0 inches. The target impedance is 55 Ω, with plus and minus fifteen percent tolerance. This maximum applies to ALL of the signals listed as 1X timing domain signals in Table 13. In addition to this maximum trace length requirement (refer to Table 16), these signals must meet the trace spacing and trace length mismatch requirements in Sections 5.3.1.2 and 5.3.1.3.

5.3.1.2. Trace Spacing Requirements

AGP 1X timing domain signals (refer to Table 13) can be routed with 5-mil minimum trace separation.

5.3.1.3. Trace Length Mismatch

There are no trace length mismatch requirements for 1X timing domain signals. These signals must meet minimum and maximum trace length requirements.

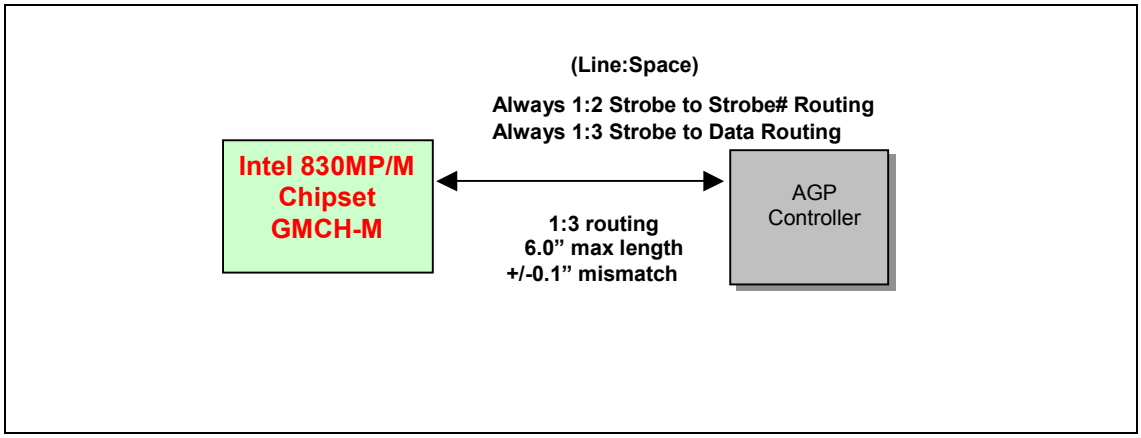
5.3.2. 2X/4X Timing Domain Routing Guidelines

5.3.2.1. Trace Length Requirements for AGP 2X/4X

These trace length guidelines apply to ALL of the signals listed as 2X/4X timing domain signals in Table 13. In addition to these maximum trace length requirements, these signals must meet the trace spacing and trace length mismatch requirements in Sections 5.3.2.2 and 5.3.2.3.

The maximum line length and mismatch requirements are dependent on the routing rules used on the motherboard. These routing rules were created to give design freedom by making tradeoffs between signal coupling (trace spacing) and line lengths. These routing rules are divided by trace spacing. In 1:2 spacing, the distance between the traces is two times the width of traces. Simulations in Mobile environment support this rule.

Figure 15. AGP Layout Guidelines



If the AGP interface is less than 6.0 inches, a 1:2 trace spacing is required for 2X/4X lines. These 2X/4X signals must be matched their associated strobe within ± 0.1 inches. This is for designs that require less than 6 inches between the graphics device and the Intel 830MP and 830M Chipset GMCH-M.

Reduce line length mismatch to ensure added margin. In order to reduce trace to trace coupling (cross talk), separate the traces as much as possible.

5.3.2.2. Trace Spacing Requirements

AGP 2X/4X timing domain signals (refer to Table 13) must be routed as documented in Table 15. They should be routed using 5-mil traces. Additionally, the signals can be routed with 5-mil spacing when breaking out of the Intel 830MP and 830M Chipset GMCH-M. The routing must widen to the requirement in Table 15 within 0.3 inches of the GMCH-M package.

Since the strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, and SB_STB#) act as clocks on the source synchronous AGP interface, special care should be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together (e.g. AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should

be routed on 5-mil traces with 10 mils of space (1:2) between them. This pair should be separated from the rest of the AGP signals (and all other signals) by at least 15 mils (1:3). The strobe pair must be length matched to less than ± 0.1 inches (that is, a strobe and its compliment must be the same length within ± 0.1 inches).

5.3.2.3. Trace Length Mismatch Requirements

The length-matching requirement depends on the maximum AGP trace length. If there are no AGP 2X/4X traces longer than 6.0 inches, then signals must be matched within ± 0.1 inches.

Table 15. AGP 2.0 Data Lengths Relative to Strobe Length

Max Trace Length	Trace Spacing	Strobe Length	Minimum Trace Length	Maximum Trace Length
< 6 in	1:2	X	X – 0.1 in	X + 0.1 in

The trace length minimum and maximum (relative to strobe length) should be applied to each set of 2X/4X timing domain signals **independently**. That is, if AD_STB0 and AD_STB0# are 5 inches, then AD[15:0] and C/BE[1:0] must be between 4.9 inches and 5.1 inches. However AD_STB1 and AD_STB1# can be 3.5 inches (and therefore AD[31:0] and C/BE#[3:2] must be between 3.4 inches and 3.6 inches). In addition, all 2X/4X timing domain signals must meet the maximum trace length requirements.

- All signals should be routed as striplines (inner layers).
- All signals in a signal group should be routed on the same layer. Routing studies have shown that these guidelines can be met. The trace length and trace spacing requirements ***must*** not be violated by any signal. Trace length mismatch for all signals within a signal group should be as close to 0 inches as possible to provide optimal timing margin.

Table 16 shows AGP 2.0 routing summary.

Table 16. AGP 2.0 Routing Guideline Summary

Signal	Maximum Length	Trace Spacing (5 mil traces)	Length Mismatch	Relative To	Notes
1X Timing Domain	6 in	10 mils	No Requirement	N/A	None
2X/4X Timing Domain Set#1	6 in	10 mils	± 0.1 in	AD_STB0 and AD_STB0#	AD_STB0, AD_STB0# must be the same length
2X/4X Timing Domain Set#2	6 in	10 mils	± 0.1 in	AD_STB1 and AD_STB1#	AD_STB1, AD_STB1# must be the same length
2X/4X Timing Domain Set#3	6 in	10 mils	± 0.1 in	SB_STB and SB_STB#	SB_STB, SB_STB# must be the same length

NOTE: Each strobe pair must be separated from other signals by at least 15 mils.

5.3.3. AGP Clock Skew

The maximum total AGP clock skew, between the Intel 830MP/830M Chipset and the graphics component, is 1 ns for all data transfer modes. This 1 ns includes skew and jitter, which originates on the motherboard, add-in module (if used), and clock synthesizer. Clock skew must be evaluated not only at a single threshold voltage, but also at all points on the clock edge that falls in the switching

range. The 1-ns skew budget is divided such that the motherboard is allotted 0.9 ns of clock skew (the motherboard designer shall determine how the 0.9 ns is allocated between the board and the synthesizer).

5.3.4. AGP Signal Noise Decoupling Guidelines

The following routing guidelines are recommended for the optimal system design. The main focus of these guidelines is to minimize signal integrity problems on the AGP interface of the Intel 830MP/830M Chipset (GMCH-M). The following guidelines are not intended to replace thorough system validation on Intel 830MP/830M Chipset-based products.

- A minimum of six 0.01-µF capacitors are required and must be as close as possible to the Intel 830MP/830M Chipset GMCH-M. These should be placed within 70 mils of the outer row of balls on the GMCH-M for VDDQ decoupling. The closer the placement, the better.
- The designer should evenly distribute placement of decoupling capacitors in the AGP interface signal field.
- Intel recommends that the designer use a low-ESL ceramic capacitor, such as with a 0603 body-type X7R dielectric.
- In order to add the decoupling capacitors within 70 mils of the Intel 830MP and 830M Chipset GMCH-M and/or close to the vias, the trace spacing may be reduced as the traces go around each capacitor. The narrowing of space between traces should be minimal and for as short a distance as possible (1 inch max.).
- In addition to the minimum decoupling capacitors, the designer should place bypass capacitors at vias that transition the AGP signal from one reference signal plane to another. On a typical four layer PCB design, the signals transition from one side of the board to the other. One extra 0.01-µF capacitor is required per 10 vias. The capacitor should be placed as close as possible to the center of the via field.

5.3.5. AGP Routing Ground Reference

Intel recommends that at least the following critical signals be referenced to ground from the Intel 830 MP/M Chipset GMCH-M to an AGP connector (or to an AGP video controller, if implemented as a "down" solution on an AGP-only motherboard), using a minimum number of vias on each net: AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, SB_STB#, G_TRDY#, G_IRDY#, G_GNT#, and ST[2:0].

In addition to the minimum signal set listed previously, Intel strongly recommends that half of all AGP signals be referenced to ground, depending on the board layout. In an ideal design, the complete AGP interface signal field would be referenced to ground. This recommendation is not specific to any particular PCB stack-up, but should be applied to all Intel 830MP and 830M Chipset designs.

5.3.6. AGP Pull-ups

The following AGP signals **do not** require pull-ups/pull-downs on the motherboard and have been integrated in the Intel 830MP/830M Chipset GMCH-M. The following signals has integrated the following pull-up resistors for the 1X Timing Domain Signals:

- FRAME#
- TRDY#
- IRDY#
- DEVSEL#
- STOP#
- RBF#
- PIPE#
- REQ#
- WBF#
- GNT#
- PAR

The following AGP strobe signals **do not** require pull-ups/pull-downs on the motherboard and have been integrated in the Intel 830MP/830M Chipset GMCH-M for the 2X/4X Timing Domain Signals are:

- AD_STB[1:0]
- SB_STB
- AD_STB[1:0]#
- SB_STB#

INTA# and INTB# should be pulled to 3.3 V, not VDDQ.

Note: G_PAR signal does not need pullup for AGP strapping option as this has integrated internally.

5.3.7. Impedance

The motherboard impedance should be controlled to minimize the impact of any mismatch between the motherboard and the add-in card. An impedance of 55 Ω ±10% is strongly recommended; otherwise, signal integrity requirements may be violated.

5.3.8. Termination

The AGP Interface does not require external *termination*.

5.4. AGP Simulation Assumptions/Estimates

The simulation methodology described below is for a post-layout design validation. It is provided for OEMs that have a post-layout simulation tool, such as ICX (Mentor Graphics*), ISIS (Viewlogic*), etc.

While layout guidelines have been developed based on a comprehensive pre-layout analysis of the technologies and simulations, OEMs are still encouraged to simulate their designs to make sure design timing and signal integrity requirements are met.

5.4.1. Assumptions/Definitions/Specifications

The source synchronous solution space consists of all designs in which the flight time mismatch between a strobe and its associated data is less than the total allowable skew:

$$T_{skew} = T_{flightdata} - T_{flightstrobe}$$

Where $T_{flightdata}$ and $T_{flightstrobe}$ are the driver-pad-to-receiver-pad flight times of the data and the strobe respectively.

The AGP physical interface is a point-to-point topology using 1.5 V or 3.3 V signaling. The baseline performance level for AGP uses a 66-MHz clock to provide a peak bandwidth of 266 MB/s. A double-clocking data technique is used to achieve twice the baseline width. Thus, AGP 2X mode provides a peak bandwidth of 533 MB/s. AGP 2X mode is a superset of the 1X mode. The AGP 4X mode clock provides high performance levels with a peak bandwidth of 1066 MB/s. This bandwidth is achieved by using a quad clocked data transfer methodology, which allows four times as much data to be transferred every 66-MHz clock cycle. AGP 4X mode is a superset of the 1X and 2X modes. Thus, all components supporting 4X must also support 1X and 2X modes.

The flight time skew simulations simulate all parameters that could cause a skew between two signals, including motherboard and add-in card line lengths, effective capacitance in the buffer models, crosstalk on each of the different interconnect combinations, data pattern dependencies, and ISI induced skews.

5.4.2. Simulation Model

A model for simulation purposes is shown in Figure 16.

Figure 16. AGP Simulations Model

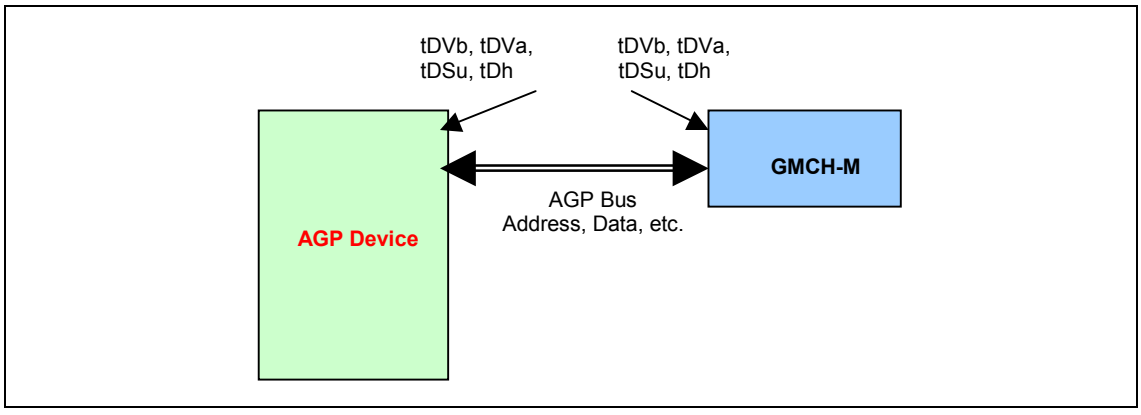
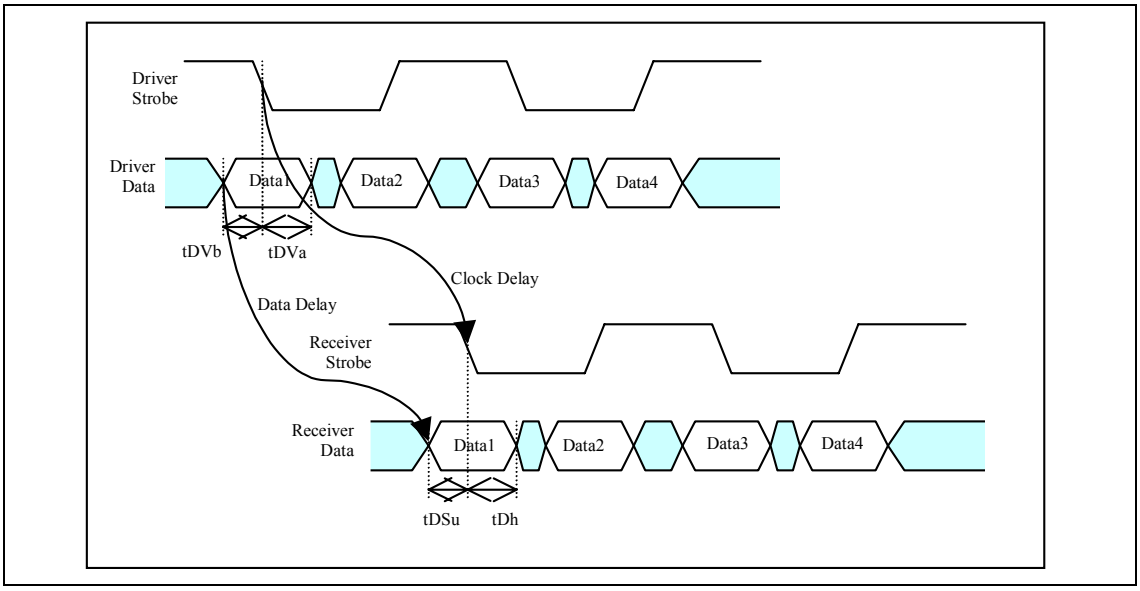


Figure 17. 4X Driver- Receiver Waveforms Relationship Specification



As shown in Figure 17, the setup margin and the hold margin for a particular design depends on the values of the data valid times and the data setup and hold times on both the driver and the receiver sides. However, note that available margins are not absolute values. Any skew due to routing and loading differences, any coupling differences in the parallel traces, and any effects of SSO (ISI, ground bounce, etc.) should be accounted for in the timing budget as they will reduce the total available margin for the design.

As an example, the timing budget that was used for Mobile 4X simulations is listed in Table 17.

Table 17. Allowable Interconnect Skew Calcuation

Component	Skew Element	Symbol	Setup	Hold	Units
Driver	Data Valid before Strobe	tDVb	950		Ps
	Data Valid after Strobe	tDVa		1150	Ps
Interconnect	Allowable Skew		550	450	Ps
Receiver	Data Setup to Strobe	tDSu	400		Ps
	Data Hold from Strobe	tDh		700	Ps

As seen in the table, total amount of skew is only 1000 psec. This skew includes allocations for SSO, crosstalk, and routing and loading introduced skew.

5.5. AGP Post-layout Validation Methodology

The simulation methodology outlined here is for post-layout validation of the AGP only. It does not apply to pre-layout analysis of the design. Although the methodology was developed using the ICX simulation tool, it was in general the goal to make the methodology applicable to other post layout tools as much as possible.

5.5.1. Define Simulation Cases Explicitly

- Simulation cases must be defined first, considering the following parameters:
- Velocity of signals, Er: Low Er:4.0 – High Er:4.4
- Characteristic impedance of boards
- Zo: 55 Ω ±15%
- Weak, typical and strong output and slow, typical and fast input buffers

Prepare models and boards as follows.

Table 18. AGP Interface Simulation Boards

Boards	GMCH-M	PCB	AGP Device
Board1	Weak Buffer IBIS	High Er and Low Zo	Slow Buffer IBIS
Board2	Weak Buffer IBIS	High Er and High Zo	Slow Buffer IBIS
Board3	Strong Buffer IBIS	Low Er and High Zo	Fast Buffer IBIS
Board4	Strong Buffer IBIS	Low Er and Low Zo	Fast Buffer IBIS
Board5	Strong Buffer IBIS	High Er and High Zo	Fast Buffer IBIS

1. Perform both READ and WRITE simulations.
   a. Enable coupled EVEN/ODD crosstalk (Board 5).
   b. Patterns with buffers switching high to low or low to high (0000 to FFFF or FFFF to 0000) or 0000 to 1110 or 1111 to 0001 or 1110 to 0001 or 0001 to 1110.
   c. Use ISI patterns (e.g.: 000001… at 266 MHz), Otherwise, allow ~ 150 ps for ISI in timing spreadsheet.
   d. For each board's specific Er, change dielectric thickness to meet Zo specified.
2. Run simulations on each board for strobe lines and also the data lines.
3. Measure flight times of all signals from Vmeas on the driver to Vmeas on the receiver.
4. Also make sure signal quality requirements are met.
5. Calculate skews between the strobe and data signals.
6. Report violations to improve routing.

5.6. AGP Power Requirements

5.6.1. AGP VDDQ and Vref

AGP specifies two separate power planes: VCC and VDDQ. VDDQ is the interface voltage. The external graphics controller may ONLY power the Intel 830MP and 830M Chipset GMCH-M AGP I/O buffers at 1.5 V. VDDQ = 3.3 V is not supported. AGP 2.0 spec requires that these power planes are separate. In conjunction with the 4X data rate, the AGP 2.0 Interface Specification provides for low-voltage (1.5 V) operation. The VCC and VDDQ power supplies are such that the VDDQ voltage level is never more than 0.5 V above the VCC voltage level.

5.6.2. Vref Generation for AGP 2.0(2X and 4X)

5.6.2.1. 1.5-V AGP Interface (AGP 2x and 4x)

In order to account for potential differences between VDDQ and GND at the Intel 830MP/830M Chipset GMCH-M and graphics controller, both devices use *source generated Vref*. That is, the Vref signal is generated at the graphics controller and *sent* to the GMCH-M and another Vref is generated at the GMCH-M and *sent* to the graphics controller.

Both the graphics controller and the GMCH-M are required to generate Vref. The voltage divider networks consist of AC and DC elements.

The Vref divider network should be placed as close to the *AGP* interface as is practical to get the benefit of the common mode power supply effects. However, the trace spacing around the Vref signals must be a minimum of 25 mils to reduce crosstalk and maintain signal integrity.

All resistors used in above reference generation schemes should have ± 1% tolerance.

5.6.3. Compensation

The Intel 830MP/830M Chipset GMCH-M AGP interface supports resistive buffer compensation (RCOMP). For Printed Circuit Boards with Characteristics impedance of 55 ohms, tie the AGP_RCOMP pin to a 54.9-Ω, 1% pull-down resistor (to ground) via a 10-mil wide, very short (≈0.5 inches) trace.

5.6.4. AGP Graphics Device Power Management Requirements

For ACPI 2.0 compliance, AGP graphics controllers are required to support the ACPI D0, D2, and D3 device states. For the ACPI D3 device power state, it is possible for AGP graphics controllers to support either a D3 HOT or D3 COLD state given certain restrictions. The D3 HOT state has often been implemented by keeping some power supplies to the graphics subsystem turned on, while the D3 COLD state has often been implemented by turning off all power supplies to the graphics subsystem. Although the ACPI 2.0 specification does not define nor differentiate between D3 HOT and D3 COLD, the Intel 830MP/830M Chipset has special requirements for D3 HOT and COLD implementations.

5.6.4.1. AGP_BUSY# Requirements for AGP Interface

The AGP_BUSY# and STP_AGP# signals allow power management signaling between an external AGP graphics controller and the ICH3-M. AGP_BUSY# indicates that the AGP device is busy. C3_STAT# (STP_AGP#) is the signal which is used for indicating to the AGP device that a C3 state transition is beginning or ending. AGP_BUSY# (ICH3-M signal) and STP_AGP# (AGP graphics controller signal) are not directly connected to the Intel 830MP/830M Chipset GMCH-M. For proper implementation, please consult Intel Field Application Engineers.

The AGP graphics device AGP_BUSY# 3.3-V signal should be pulled up to 3-V switched rail, the power rail that is powered OFF during S3.

5.6.4.2. Supported D3 HOT Implementations

Due to potential long-term reliability issues, only D3 HOT implementations where there is no leakage or non-zero voltage driven into the Intel 830MP and 830M Chipset GMCH-M are supported.

5.6.4.3. Supported D3 COLD Implementations

In the D3 COLD device state, the AGP Vddq rail and the all other graphics subsystem rails are turned off. In this device state, the video memory and context will be lost unless it is saved in a secondary storage device. D3 COLD is the recommended D3 device state to implement due to power savings.

6. Integrated Graphics Display Port

The Intel 830M and 830MG Chipset GMCH-M contains four display ports, an analog RAMDAC and three 12-bit Digital Video Out (DVO) devices. Section 6.1 will discuss the CRT and RAMDAC routing requirements. Section 6.2 will discuss the dedicated DVOA port. Section 6.3 will discuss the DVOB and DVOC design guideline. Section 6.4 provides recommendations for a flexible modular design guideline for the AGP and the DVOB/DVOC muxed interface. Section 6.5 provides recommendations for the GPIO signal group.

6.1. Analog RGB/CRT Guidelines

6.1.1. RAMDAC/Display Interface

The Intel 830M and 830MG Chipset integrated graphics/chipset design interfaces to an analog display via a RAMDAC. The RAMDAC is a subsection of the graphics controller display engine and consists of three identical 8-bit digital-to-analog converter (DAC) channels, one for the display's red, green, and blue electron guns.

Each RGB output is doubly terminated with a 75-Ω resistance: One 75-Ω resistance is connected from the DAC output to the board ground, and the other termination resistance exists within the display. The equivalent DC resistance at the output of each DAC is 37.5 Ω. The current output from each DAC flows into this equivalent resistive load to produce a video voltage, without the need for external buffering. There is also an LC pi-filter on each channel that is used to reduce high-frequency noise and to reduce EMI. In order to maximize the performance, the filter impedance, cable impedance, and load impedance should be matched.

6.1.2. Reference Resistor (Rset)

A reference resistor, R_{set}, is used to set the reference current for the DAC. This resistor is an external resistor with a 1% tolerance that is placed on the circuit board.

A reference voltage is generated on the Intel 830M and 830MG Chipset GMCH-M from a bandgap voltage reference circuit. The bandgap reference voltage level is approximately 1.2 V and this voltage reference is divided in two to generate the reference voltage. The VESA video standard defines the LSB current for each DAC channel. The RAMDAC reference current is designed on-die to be equal to 32LSB.

Therefore, the external reference resistor value is defined as:

Equation 1. R_{SET} Equation

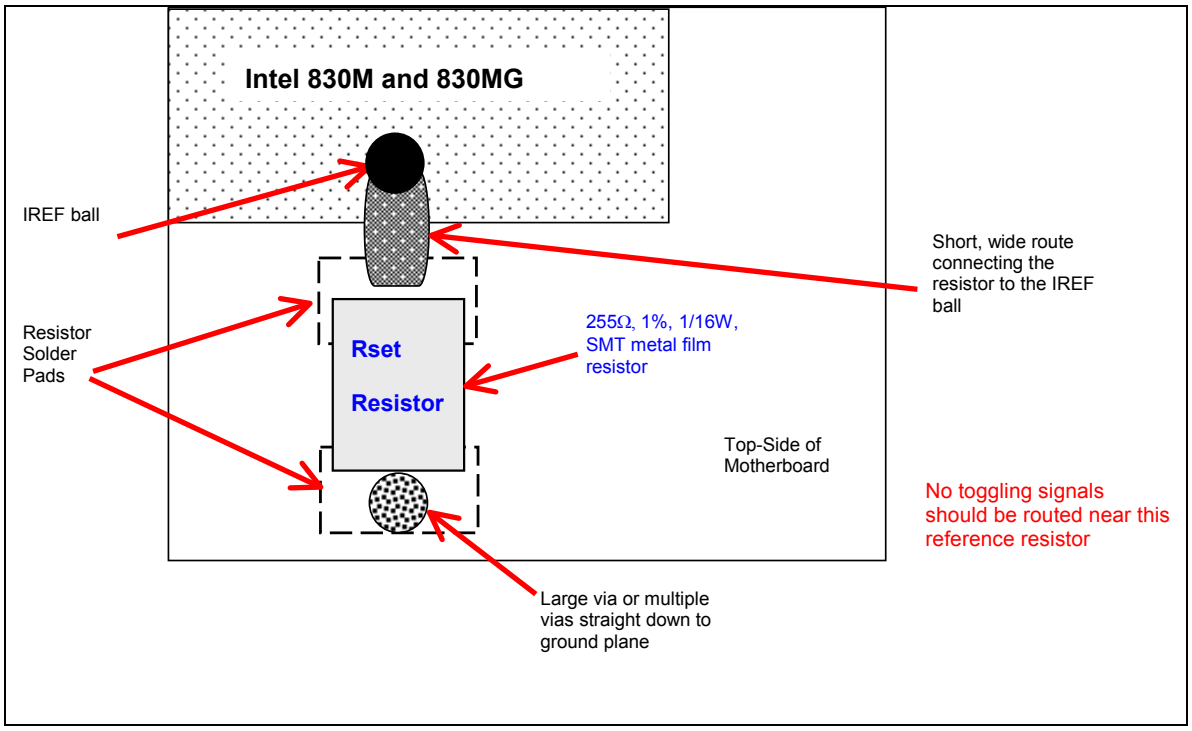
$$Rset = \frac{Vreference}{Ireference} = \frac{(Vbg/2)}{32*(73.2uA)} = 256\Omega$$

Resistor values of 249 Ω, 255 Ω, and 261 Ω are standard 1% precision resistor values.

Recommended Intel 830M and 830MG Chipset GMCH-M DAC Reference Resistor			
Value	**Tolerance**	**Power**	**Type**
255 Ω	1%	1/16 W	SMT, Metal Film

The recommended placement and layout of this reference resistor is shown in Figure 18.

Figure 18. Rset Placement



6.1.3. RAMDAC Board Design Guidelines

In order for the DAC to successfully run at speeds up to 350 MHz, care should be taken when routing the analog RAMDAC signals. Intel recommends that each analog R, G, B signal be routed differentially with its complement signal R#,G#,B#. A pair (i.e. red and red#) should be routed 75-Ω, odd-mode differential. This equates to ~10 mil trace for both traces with as little space (~5 mils) between the pair as possible. Spacing between pairs and to other signals should be maximized, 20-mil spacing is recommended. The RGB signals require pi filters that should be placed near the VGA connector. It consists of two 3.3-pF caps with a 75 Ω at 100-MHz FB between them. Prior to hitting this filter, the RGB signals should have a 75 Ω 1% terminating pull-down resistor. The complement signals (R#, G#, and B#) do not require a pi filter and should be terminated with a ~37.5-Ω, 1% resistor to ground.

Each analog signal should be matched to its complement as closely as possible. This includes the routing channel for each signal as well as the loading on that signal. Also, the three pairs (R/R# combined) should closely resemble each other. If possible, try to match bends in one pair to the other two.

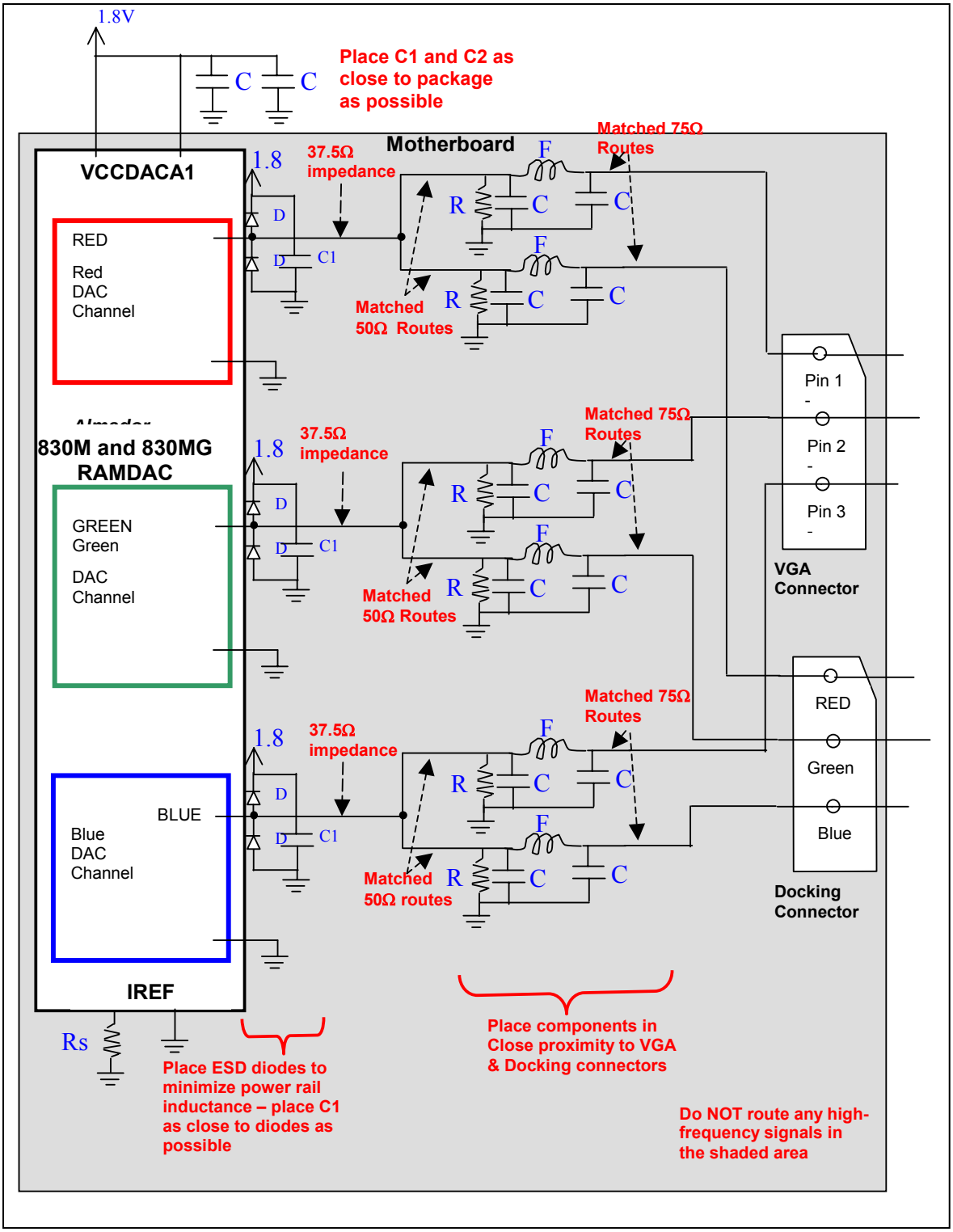
Signals within a pair should be routed with 5-mil spacing for as long a length as possible. To accomplish this, Intel recommends that the pi filter and terminating resistors be placed as close as possible to the VGA connector. The complement signals should terminate through their 37.5- Ω resistors at the same location that the RGB signals hit their 75- Ω terminating resistors. After hitting their 75- Ω terminating resistors, the RGB signals should continue on to their pi filters and the VGA connector, *but should now ideally be routed with a 75-Ohm impedance (~ 5 mil traces).* In order to have the complements' loading and edge rates more closely resemble that of the RGB signals, the complements may have a capacitor across their terminating resistors to mimic the pi filter.

The RGB signals also require protection diodes between 1.8 V and ground. These diodes should have low C ratings (~5 pF max) and small leakage current (~ 10 µA at 120˚C) and should be properly decoupled with a 0.1-µF cap. These diodes and decoupling should be placed to minimize power rail inductance. In order to have the complements' loading more closely resemble that of the RGB signals, the complements may have similar diodes. The choice between diodes (or diode packs) should comprehend the recommended electrical characteristics in addition to cost.

The RGB signals should be length matched as closely as possible (from the Intel 830M and 830MG Chipset GMCH-M to VGA connector) and should not exceed 200 mils of mismatch.

6.1.4. Intel 830M and 830MG Chipset DAC Routing Guidelines With Docking Connector

Figure 19. Intel 830M and 830MG Chipset DAC Routing Guidelines With Docking Connector



6.1.5. DAC R, G, B Termination Resistors

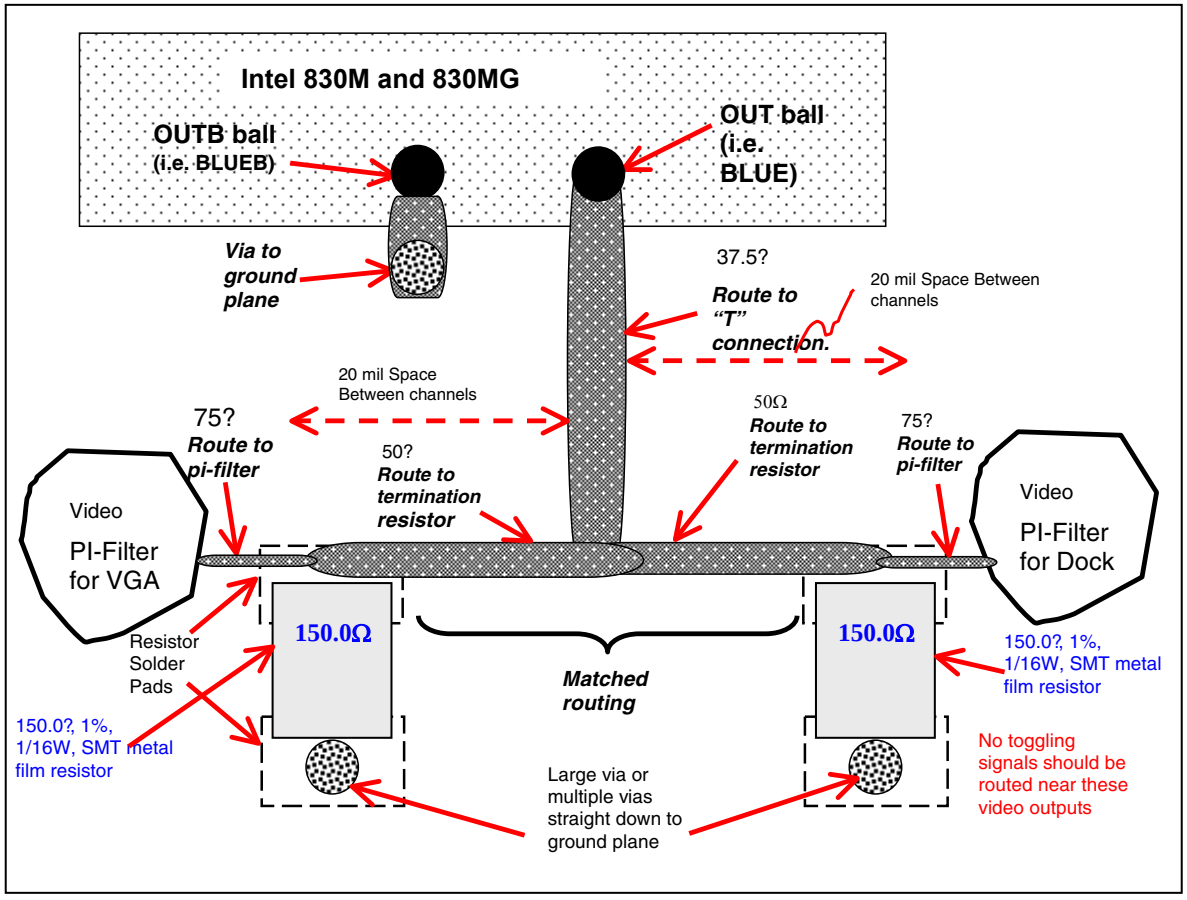
The Intel 830M and 830MG Chipset DAC channel (red, green, blue) outputs are routed as single-ended shielded current output routes that are terminated prior to connecting to the video PI-filter and VGA/docking connector.

Table 19. Recommended Intel 830M and 830MG Chipset DAC R,G,B Termination Resistors for Mobile Board Designs for Docking Connector Support

Value	Tolerance	Power	Type
150.0 Ω	1%	1/16 W	SMT, Metal Film

The recommended routing of the termination resistors is shown in the following figure. The RED, GREEN, and BLUE output routes should be routed as a 50-Ω impedance from the T-route point to each termination resistor.

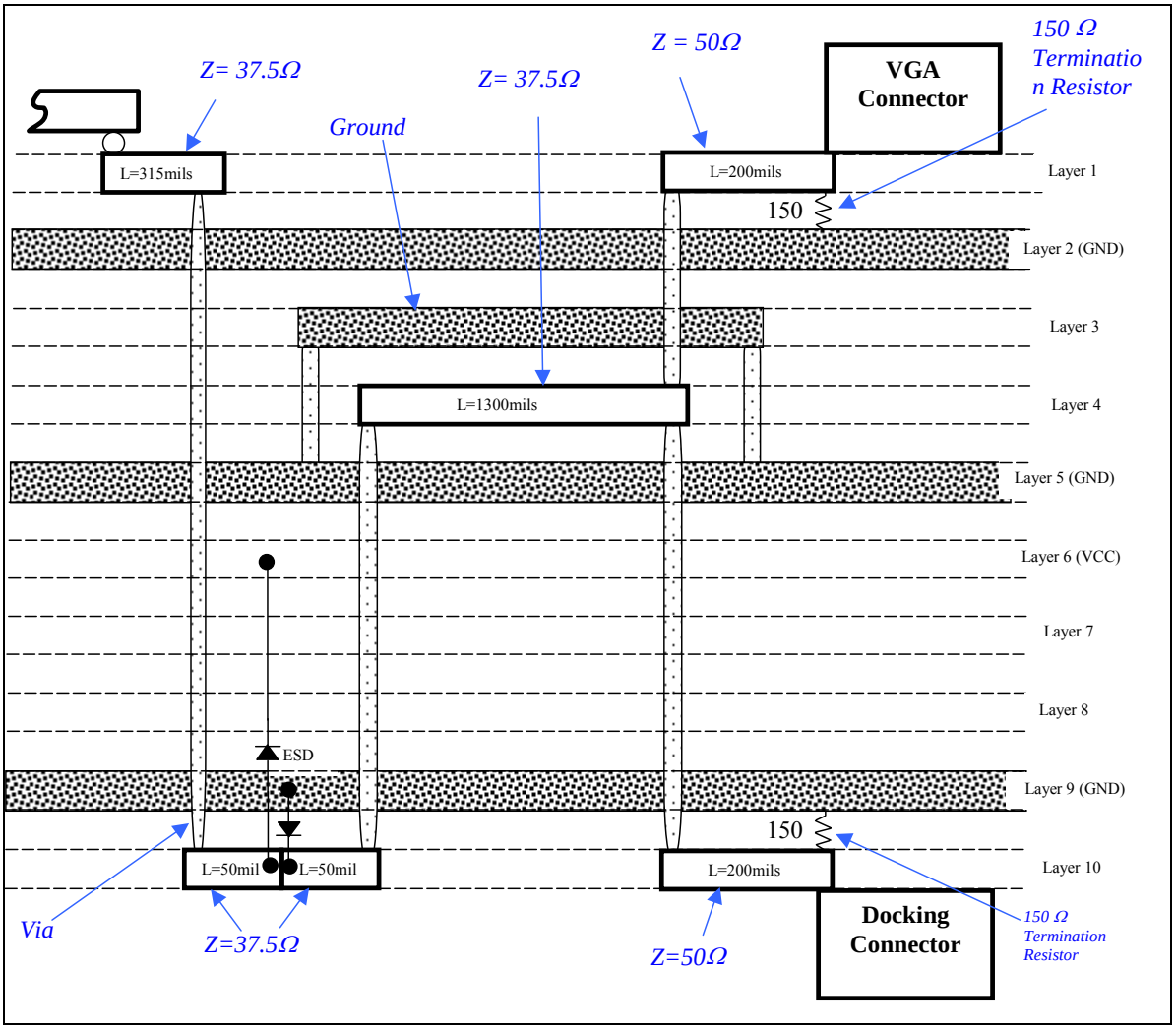
Figure 20. Recommended DAC R, G, B Output Routing and Termination Resistor Layout (Only One Channel is Illustrated)



6.1.6. Intel 830M and 830MG Chipset GMCH-M DAC Routing/Stackup Example

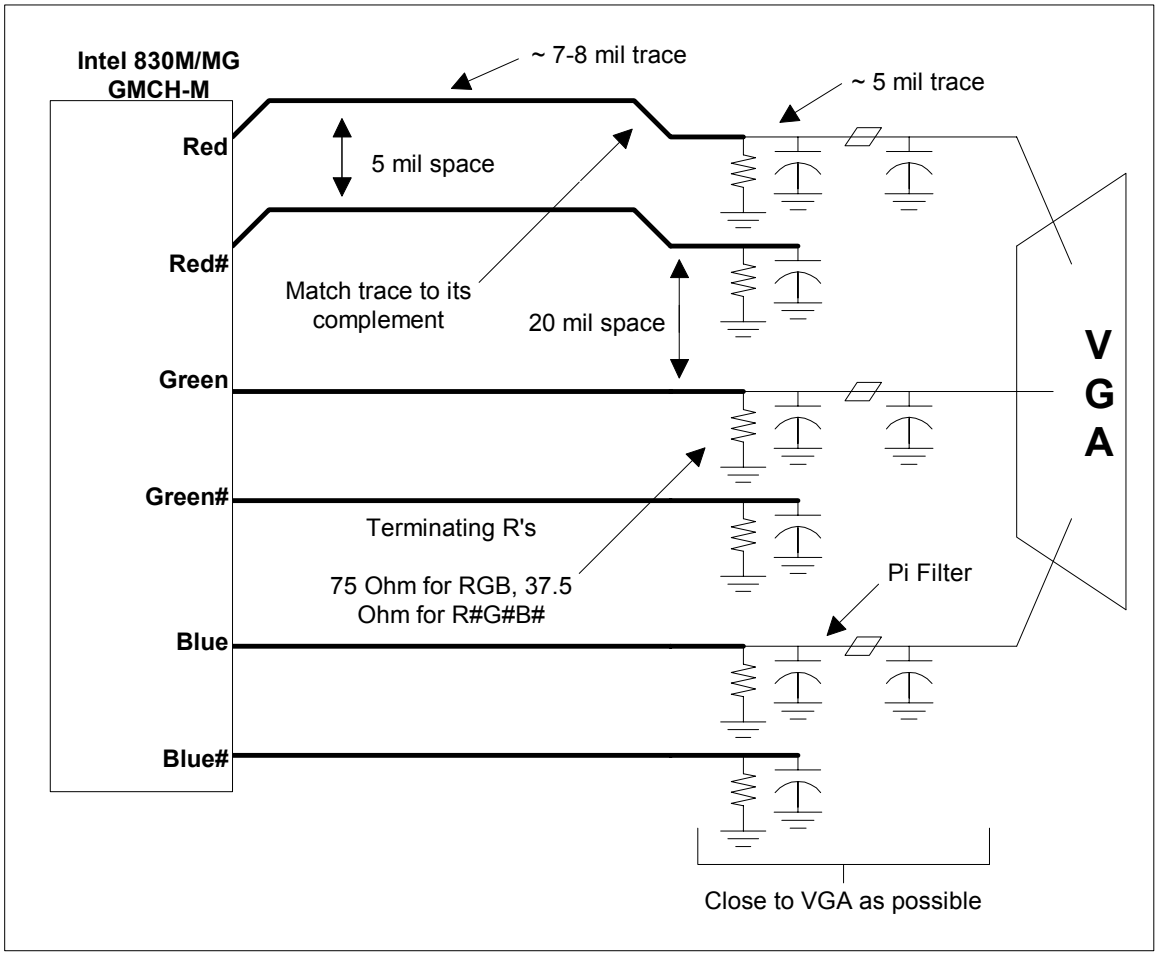
An example Intel 830M and 830MG Chipset GMCH-M DAC routing for a mobile board design is shown in the figure below. Mobile board designs usually require the DAC to drive either a VGA connector or a docking station connector. The figure shows a typical cross-section view of a mobile board design showing an example of recommended GMCH-M DAC routing (one DAC channel, pi-filter components not shown – not to scale).

Figure 21. Recommended DAC Routing/Stackup Example for VGA and Docking Connector



6.1.7. Intel 830M and 830MG Chipset DAC Routing Guidelines Without Docking Connector

Figure 22. Intel 830M and 830MG Chipset DAC Routing Guidelines Without Docking Connector



NOTE: This figure does not illustrate the required diodes.

Table 20. Recommended Intel 830M and 830MG Chipset GMCH-M DAC R#, G#, B# Termination Resistors for Mobile Board Designs for Non-Docking Connector Support

Value	Tolerance	Power	Type
37.5 Ω	1%	1/16 W	SMT, Metal Film

6.1.8. DAC Power Requirements

The DAC requires a 1.8-V supply through its two VCCA_DAC balls. The two may share a set of capacitors, 0.1 µF and 0.01 µF, but this connection should have low inductance. Separate analog power or ground planes are not required for the DAC.

6.1.9. HSYNC, VSYNC, and DDC1 Considerations

These are 3.3-V outputs from the Intel 830M and 830MG Chipset GMCH-M, if higher signaling voltages are needed (5 V), level-shifting devices will be required. DDC1DATA and DDC1CLK should be connected to the analog display attached to the DAC. 4.7-kΩ pull-ups (or pull-ups with the appropriate value derived from simulation) are required on each of these signals. These signals are 3.3-V tolerant. If higher signaling voltages are needed (5 V), then level-shifting devices will be required. See Section 6.5 for further pullup recommendations for the DDC1 (GPIO) signal group.

6.2. Digital Video Out (DVOA) Interface

Intel 830M and 830MG Chipset GMCH-M's dedicated Digital Video Out Port A (DVOA) is a 1.5-volt interface that can support transactions up to 165 MHz. The Intel DVO port interface supports a wide variety of DVO compliant devices (e.g. discrete TV encoder, discrete TMDS transmitter, combination TV encoder and TMDS transmitter or LVDS transmitters).

6.2.1. DVOA Interface Signal Groups

The DVO interface signals include:

- Input Signals
  - DVOA_CLKINT
  - DVOA_FLD/STL
  - DVOA_INTR#
- Output Data Signals
  - DVOHSYNC
  - DVOVSYNC
  - DVOBLANK#
  - DVOA_DATA[11:0]
- Output Strobe Signals
  - DVOA_CLK
  - DVOA_CLK#

6.2.2. DVOA Interface Routing Guidelines

6.2.2.1. DVOA Trace Spacing and Trace Length Mismatch Requirements

Route data signals (DVOA_Data[11:0]) with a trace width of *5* mils and a trace spacing of *10* mils. These signals can be routed with a trace width of *5* mils and a trace spacing of *10* mils for navigation around components or mounting holes. In order to break out of the Intel 830M and 830MG Chipset GMCH-M, the DVOA data signals can be routed with a trace width of *5* mils and a trace spacing of *5* mils. The signals should be separated to a trace width of *5* mils and a trace spacing of *10* mils within 0.3 inches of the GMCH-M component. The maximum trace length for the DVOA data signals is 6 inches. These signals should each be matched within ± 0.1 inch of the DVOA_CLKOUT[1:0] signals.

Route the DVOA_CLKOUT[1:0] signals 5 mils wide and 10 mils apart. This signal pair should be a minimum of 10 mils from any adjacent signals. The maximum length for DVOA_Clkout[1:0] is 6.0 inches, and the two signals should be the same length.

All signals should be routed as striplines (inner layers).

All signals in a signal group should be routed on the same layer. Routing studies have shown that these guidelines can be met. The trace length and trace spacing requirements ***must*** not be violated by any signal. Trace length mismatch for all signals within a signal group should be as close to 0 inches as possible to provide optimal timing margin.

Table 21 shows DVOA routing summary.

Table 21. DVOA Routing Guideline Summary

Signal	Maximum Length	Trace Spacing (5 mil traces)	Length Mismatch	Relative To	Notes
DVOA_data [11:0]	6 in	10 mils	± 0.1 in	DVOA_Clkout	DVOA_Clkout [1:0] must be the same length

Each strobe pair must be separated from other signals by at least 15 mils. For DVO interface and multixed design, more conservative length mismatch (± 0.1 inch) is adopted.

6.2.2.2. DVOA Impedance

The motherboard impedance should be controlled to minimize the impact of any mismatch. An impedance of 55 Ω ± 15 % is strongly recommended; otherwise, signal integrity requirements may be violated.

6.2.2.3. DVOA Termination

The DVO interface does not require external termination.

6.2.3. DVOA Assumptions/Definitions/Specifications

The source synchronous solution space consists of all designs in which the flight time mismatch between a strobe and its associated data is less than the total allowable skew:

$$\mathbf{T}_{skew} = \mathbf{T}_{\mathbf{flight}data} - \mathbf{T}_{\mathbf{flight}strobe}$$

Where $\mathbf{T}_{\mathbf{flight}data}$ and $\mathbf{T}_{\mathbf{flight}strobe}$ are the driver-pad-to-receiver-pad flight times of the data and the strobe respectively.

The DVO physical interface is a point-to-point topology using 1.5-V signaling. The DVO uses a 165-MHz clock.

The flight time skew simulations simulate all parameters that could cause a skew between two signals, including motherboard and add-in card line lengths, effective capacitance in the buffer models, crosstalk on each of the different interconnect combinations, data pattern dependencies, and ISI induced skews.

6.2.4. DVOA Simulation Method

A model for simulation purposes is shown in Figure 23. The DVO component is a third party-chip.

Figure 23. DVOA Simulations Model

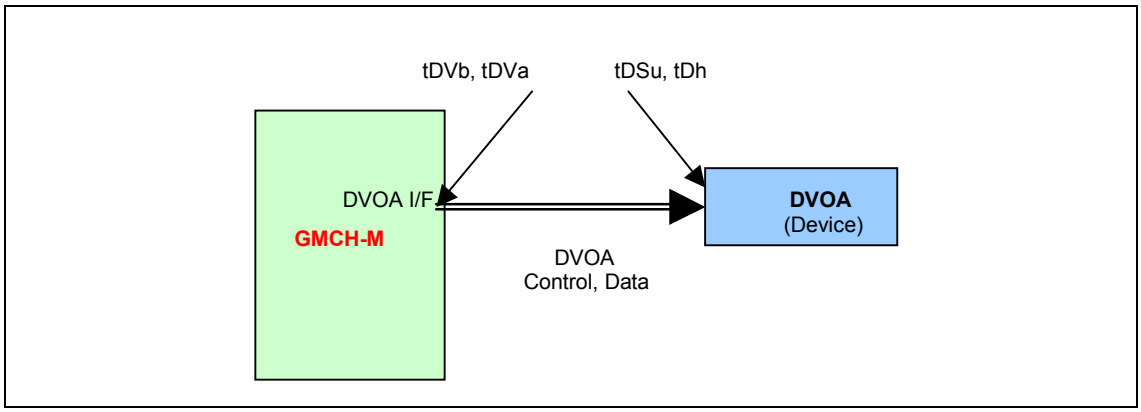
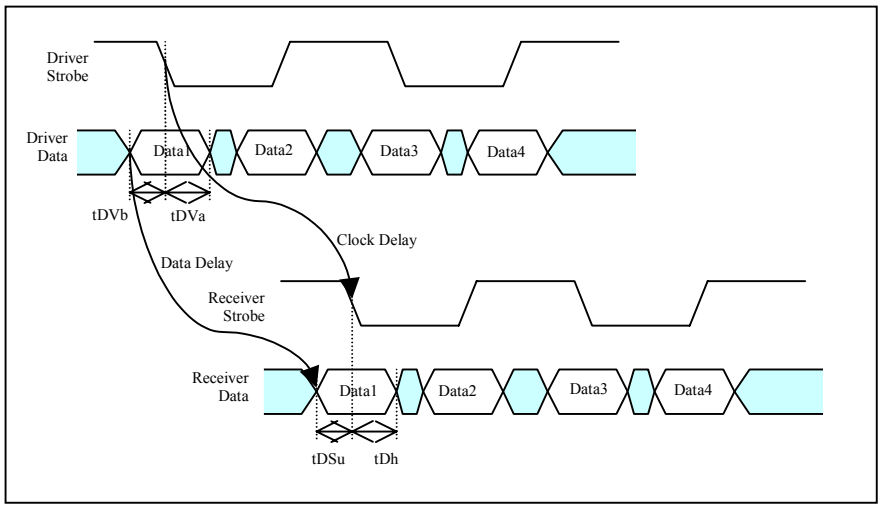


Figure 24. Driver-Receiver Waveforms Relationship Specification



The setup margin and the hold margin for a particular design depends on the values of the data valid times and the data setup and hold times on both the driver and the receiver sides. However, note that available margins are not absolute values. Any skew due to routing and loading differences, any coupling differences in the parallel traces, and any effects of SSO (ISI, ground bounce, etc.) should be accounted for in the timing budget as they will reduce the total available margin for the design.

Table 22. Allowable Interconnect Skew Calcuation

Component	Skew Element	Symbol	Setup	Hold	Units
Driver	Data Valid before Strobe	tDVb	570		ps
	Data Valid after Strobe	tDVa		770	ps
Interconnect	Allowable Skew		320	520	ps
Receiver	Data Setup to Strobe	tDSu	250		ps
	Data Hold from Strobe	tDh		250	ps

All numbers in this table are from the Intel 830M and 830MG Chipset GMCH-M specification documents that are applicable for this interface.

6.2.5. DVOA Post-layout Validation Methodology

The simulation methodology outlined here is for post-layout validation of the DVO only and does not apply to pre-layout analysis of the design. Although the methodology was developed using the ICX simulation tool, it was in general the goal to make the methodology applicable to other post layout tools as much as possible.

6.2.5.1. Define Simulation Cases Explicitly

Simulation cases must be defined first, considering the following parameters:

1. Velocity of signals, Er: Low Er:4.0 – High Er:4.4
2. Characteristic impedance of boards: Zo: 55 Ω ± 15%
3. Weak, typical and strong output and slow, typical and fast input buffers

Prepare models and boards as follows:

Table 23. DVOA Interface Simulation Boards

Boards	GMCH-M	PCB	DVO Device
Board1	Weak Buffer IBIS	High Er and Low Zo	Slow Buffer IBIS
Board2	Weak Buffer IBIS	High Er and High Zo	Slow Buffer IBIS
Board3	Strong Buffer IBIS	Low Er and High Zo	Fast Buffer IBIS
Board4	Strong Buffer IBIS	Low Er and Low Zo	Fast Buffer IBIS
Board5	Strong Buffer IBIS	High Er and High Zo	Fast Buffer IBIS

1. Perform both READ and WRITE simulations.
   a. Enable coupled EVEN/ODD crosstalk (Board 5).
   b. Patterns with buffers switching high to low or low to high (0000 to FFFF or FFFF to 0000) or 0000 to 1110 or 1111 to 0001 or 1110 to 0001 or 0001 to 1110.
   c. Use ISI patterns (e.g.: 000001… at 165 MHz), Otherwise, allow ~ 150 ps for ISI in timing spreadsheet.
   d. For each board's specific Er, change dielectric thickness to meet Zo specified.
2. Run simulations on each board for strobe lines and also the data lines.
3. Measure flight times of all signals from Vmeas on the driver to Vmeas on the receiver.
4. Also make sure signal quality requirements are met.
5. Calculate skews between the strobe and data signals.
6. Report violations to improve routing.

6.3. DVOB and DVOC Interface

6.3.1. AGP/DVO Muxed Interface (830M Only)

As described previously, the AGP interface of the Intel 830M Chipset is multiplexed or shared with the DVOB and DVOC interfaces. In other words, the same component pins (balls) are used for both interfaces, although obviously only one interface can be supported at any given time. As a result, all DVOB and DVOC interface signals are mapped onto the AGP interface.

In the AGP mode, the interface supports a full AGP 4X interface. In DVO mode, the interface becomes a digital display interface similar to the dedicated DVO (DVOA). The main difference between the multiplexed interface and the dedicated DVO is that the multiplexed digital display interface can run in dual-channel mode. This provides an effective pixel clock up to twice that supported by the dedicated DVO (nearly 330 MHz compared to 165 MHz). This allows the Intel 830M Chipset to support digital displays with higher resolutions and refresh rates.

6.3.2. DVOB and DVOC Interface Routing Guidelines

6.3.2.1. Trace Spacing and Trace Length Mismatch Requirements

The routing guidelines for the multiplexed DVOB and DVOC interfaces are the same as for the DVOA interface.

Table 24 shows the multiplexed DVOB and DVOC interface routing summary.

Table 24. DVOB and DVOC Interface Routing Guideline Summary

Signal	Maximum Length	Trace Spacing (5 mil traces)	Length Mismatch	Relative To	Notes
DVOB and DVOC Data [11:0]	6 in	10 mils	± 0.1 in	DVO_Clkout	

Each strobe pair must be separated from other signals by at least 15 mils. For multiplexed design, more conservative length mismatch (± 0.1 in) is adopted.

6.3.3. DVOB and DVOC Assumptions/Definitions/Specifications

The source synchronous solution space consists of all designs in which the flight time mismatch between a strobe and its associated data is less than the total allowable skew:

$$\mathbf{T}_{skew} = \mathbf{T}_{\mathbf{flight}data} - \mathbf{T}_{\mathbf{flight}strobe}$$

Where $\mathbf{T}_{\mathbf{flight}data}$ and $\mathbf{T}_{\mathbf{flight}strobe}$ are the driver-pad-to-receiver-pad flight times of the data and the strobe respectively.

The DVO physical interface is a point-to-point topology using 1.5-V signaling. The Intel 830M and 830MG Chipset DVO interfaces supports up to a 165-MHz clock.

The flight time skew simulations simulate all parameters that could cause a skew between two signals, including motherboard and add-in card line lengths, effective capacitance in the buffer models, crosstalk on each of the different interconnect combinations, data pattern dependencies, and ISI induced skews.

6.3.4. DVOB and DVOC Simulation Method

A model for simulation purposes is shown in Figure 25.

Figure 25. DVOB and DVOC Simulations Model

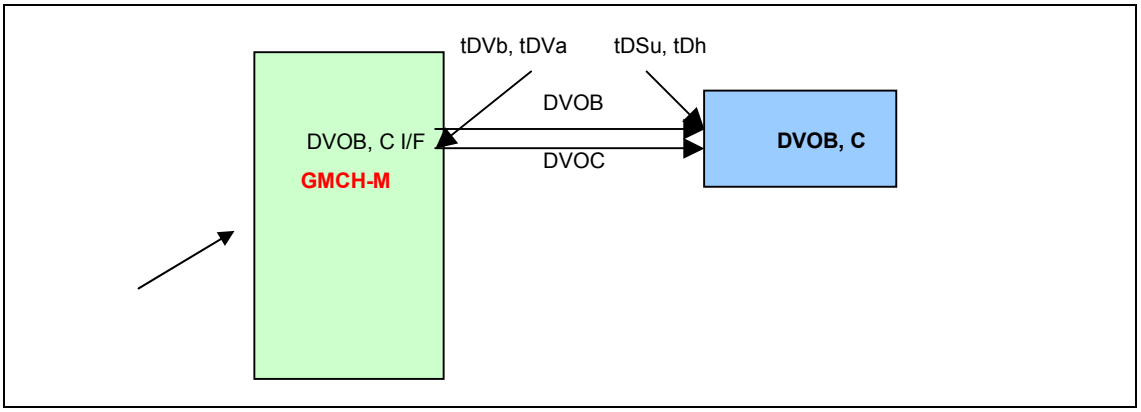
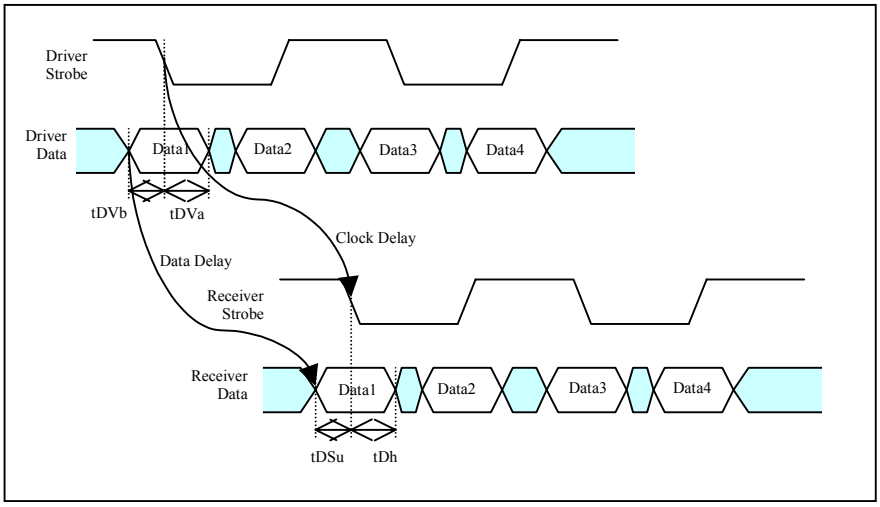


Figure 26. Driver-Receiver Waveforms Relationship Specification



The setup margin and the hold margin for a particular design depends on the values of the data valid times and the data setup and hold times on both the driver and the receiver sides. However, note that available margins are not absolute values. Any skew due to routing and loading differences, any coupling differences in the parallel traces, and any effects of SSO (ISI, ground bounce, etc.) should be accounted for in the timing budget as they will reduce the total available margin for the design.

Table 25. Allowable Interconnect Skew Calcuation

Component	Skew Element	Symbol	Setup	Hold	Units
Driver	Data Valid before Strobe	tDVb	570		ps
	Data Valid after Strobe	tDVa		770	ps
Interconnect	Allowable Skew		320	520	ps
Receiver	Data Setup to Strobe	tDSu	250		ps
	Data Hold from Strobe	tDh		250	ps

All numbers in this table are from the Intel 830 Chipset family GMCH-M specification documents that are applicable for this interface.

6.3.5. DVOB and DVOC Post-layout Validation Methodology

The simulation methodology outlined here is for post-layout validation of the DVO only. It does not apply to pre-layout analysis of the design. Although the methodology was developed using the ICX simulation tool, it was in general the goal to make the methodology applicable to other post layout tools as much as possible.

6.3.5.1. Define Simulation Cases Explicitly

Simulation cases must be defined first, considering the following parameters:

Velocity of signals, Er: Low Er:4.0 – High Er:4.4

Characteristic impedance of boards: Zo: 55 Ω ± 15%

Weak, typical and strong output and slow, typical and fast input buffers

Prepare models and boards as follows:

Table 26. DVO Interface Simulation Boards

Boards	GMCH-M	PCB	DVO Device
Board1	Weak Buffer IBIS	High Er and Low Zo	Slow Buffer IBIS
Board2	Weak Buffer IBIS	High Er and High Zo	Slow Buffer IBIS
Board3	Strong Buffer IBIS	Low Er and High Zo	Fast Buffer IBIS
Board4	Strong Buffer IBIS	Low Er and Low Zo	Fast Buffer IBIS
Board5	Strong Buffer IBIS	High Er and High Zo	Fast Buffer IBIS

1. Perform both READ and WRITE simulations.
   a. Enable coupled EVEN/ODD crosstalk (Board 5).
   b. Patterns with buffers switching high to low or low to high (0000 to FFFF or FFFF to 0000) or 0000 to 1110 or 1111 to 0001 or 1110 to 0001 or 0001 to 1110.

c. Use ISI patterns (e.g.: 000001… at 165 MHz), Otherwise, allow ~ 150 ps for ISI in timing spreadsheet.

d. For each board's specific Er, change dielectric thickness to meet Zo specified

2. Run simulations on each board for strobe lines and also the data lines.
3. Measure flight times of all signals from Vmeas on the driver to Vmeas on the receiver.
4. Also make sure signal quality requirements are met.
5. Calculate skews between the strobe and data signals.
6. Report violations to improve routing.

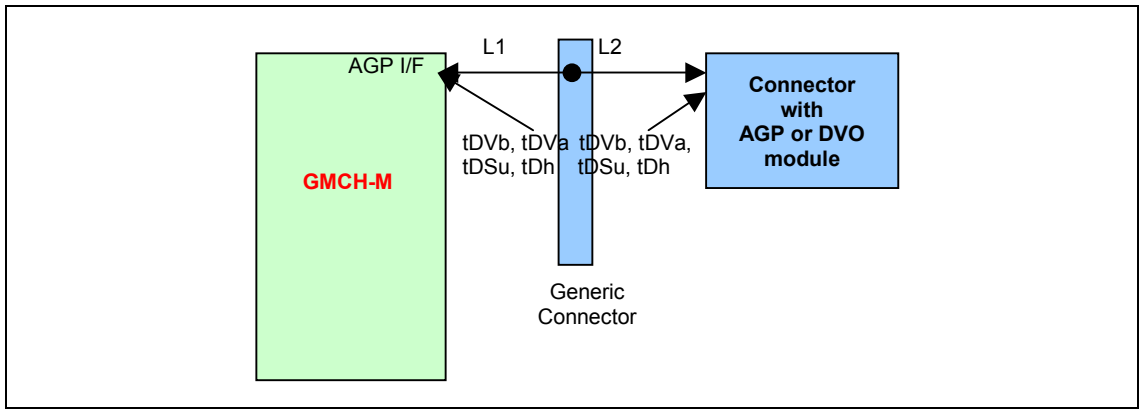
6.4. AGP and DVO Flexible (Modular) Design

The Intel 830M Chipset GMCH-M supports flexible design interfaces described in this section.

6.4.1. The Intel 830M Chipset GMCH-M AGP/DVO Module Design

The Intel 830M chipset GMCH-M supports either an AGP device or a DVO module design connected to the GMCH-M through a generic connector. The GMCH-M will then behave as both driver and receiver. The Q-switch is disabled in this case. Simulation method is the same as in Section 3. Lengths L1 and L2 are determined by simulation as L1= 4 inches and L2= 2 inches. Refer to Figure 27 for the generic connector parasitic model.

Figure 27. AGP Enabled Simulation Model



All signals should be routed as striplines (inner layers).

All signals in a signal group should be routed on the same layer. Routing studies have shown that these guidelines can be met. The trace length and trace spacing requirements ***must*** not be violated by any signal. Trace length mismatch for all signals within a signal group should be as close to ± 0.1 inches as possible to provide optimal timing margin.

Table 27 shows AGP enabled routing guideline summary.

Table 27. AGP Enabled Routing Guideline Summary

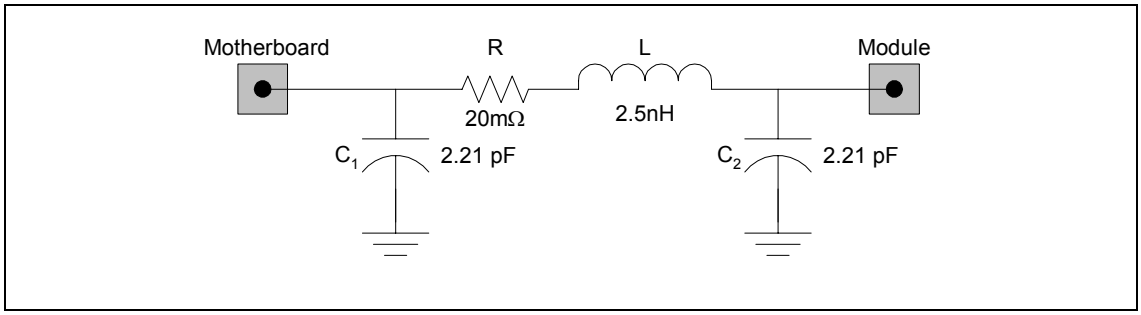
Signal	Maximum Length	Trace Spacing (5 mil traces)	Length Mismatch	Relative To	Notes
AGP 2X/4X Timing Domain	L1=4 in L2=2 in	10 mils	± 0.1 in		

For DVO module case, the simulation model is the same as Figure 27 and the routing guideline is the same as in Table 27; 1-each strobe pair must be separated from other signals by at least 15 mils. For multiplexed design, more conservative length mismatch (± 0.1 inches) is adopted.

6.4.1.1. Generic Connector Model

Table 28 shows the generic connector model used in simulation for flexible AGP/DVO implementation. This is only for reference. Actual connector may have different parasitic values. Designs using this approach need to be simulated first.

Table 28. Generic Module Connector Parasitic Model



6.5. DVOA/DVOB/DVOC GMBUS and DDC Interface Considerations

The Intel 830M and 830MG Chipset GMCH-M DVOA, DVOB and DVOC ports control the video front-end devices via the GMBUS (I2C) interface. The Intel 830M and 830MG Chipset GMCH-M has 5 GMBUS pairs that can be used in any combination of DVO ports (DVOA, DVOB or DVOC). The protocol and bus are used to configure registers in the TV encoder, TMDS/LVDS transmitter chips and the Intel VCH chip. The GMCH-M also has an option to utilize the DDC2CLK and DDC2DATA to collect EDID (Extended Display Identification) from a digital display panel.

The GMBUS should be connected to the DVO device, as required by the specifications for those devices. DDC1_DATA and DDC1_CLK should be connected to the CRT connector. DDC2_DATA and DDC2_CLK should be connected to the DVI connector, as specified by the DVI specification. Typically 4.7-kΩ - 10 kΩ pull-ups (or pull-ups with the appropriate value derived from simulating the signal) are required on each of these signals.

The following 830M GMCH-M signal groups list the five possible GMBUS pairs.

- DDC1_CLK / DDC1_DATA
- I2C_CLK / I2C_DATA
- DDC2_CLK / DDC2_DATA

- M_I2C_CLK (G_IRDY#) / M_I2C_DATA (G_DEVSEL#)
- M_DDC1_CLK (G_TRDY#) / M_DDC1_DATA (G_FRAME#)

If any of the five GMBUS pairs signals are not used; 4.7 K – 100 KΩ pull-up (or pull-ups with the appropriate value derived from simulating the signal) resistors are required. This will prevent the GMCH-M DVOA interface from confusing noise on these lines for false cycles.

If muxed DVOs are being used, please note that G_PAR should be pulled down to ground on the platform using a 330-Ωresistor.

6.5.1. Leaving the Intel 830M and 830MG Chipset GMCH-M DVOA, DVOB, or DVOC Port Unconnected

If the motherboard does not implement any of the possible video devices with the DVOA port, please follow the recommenced guidelines recommended on the motherboard:

- DVOA Output signals may be left unconnected if they are not used.
  - Pull-up resistors are required for the following signals:
    - DVOA_INTR#
    - DVOA_CLKINT
  - Pull-down resistors are required for the following signals:
    - DVOA_FLD/STALL
- Route the following signals out of the BGA to test points for use by automated test equipment (if required). These signals are part of one of the Intel 830M and 830MG Chipset GMCH-M XOR chains.
  - DVOA_D[11:0]
  - DVOA_CLK
  - DVOA_CLK#
- DVOB or DVOC Output signals may be left unconnected if they are not used.
  - Pull-down resistors are required for the following signals if not used:
    - DVOB_FLD / STL / G_AD14
    - DVOC_FLD/ STL / G_AD31
  - Pull-up resistors are required for the following signals if not used:
    - DVOBC_CLKINT
    - DVOBC_INTR#/DPMS_CLK

If muxed DVOs are being used, please note that G_PAR should be pulled down to ground on the platform using a 330-Ω resistor.

7. Intel 830 Chipset Family GMCH-M PLL Requirements

The Intel 830 Chipset family GMCH-M contains four different phase-locked loop circuits on the same die. There is a Host PLL (HPLL), a Core PLL (CPLL) and two display PLLs (DPLLA and DPLLB). The HPLL, CPLL and DPLL [A:B] require standard de-coupling capacitance.

7.1. Intel 830 Chipset Family GMCH-M PLL Filter Design Guidelines

7.1.1. Host and Core PLLs

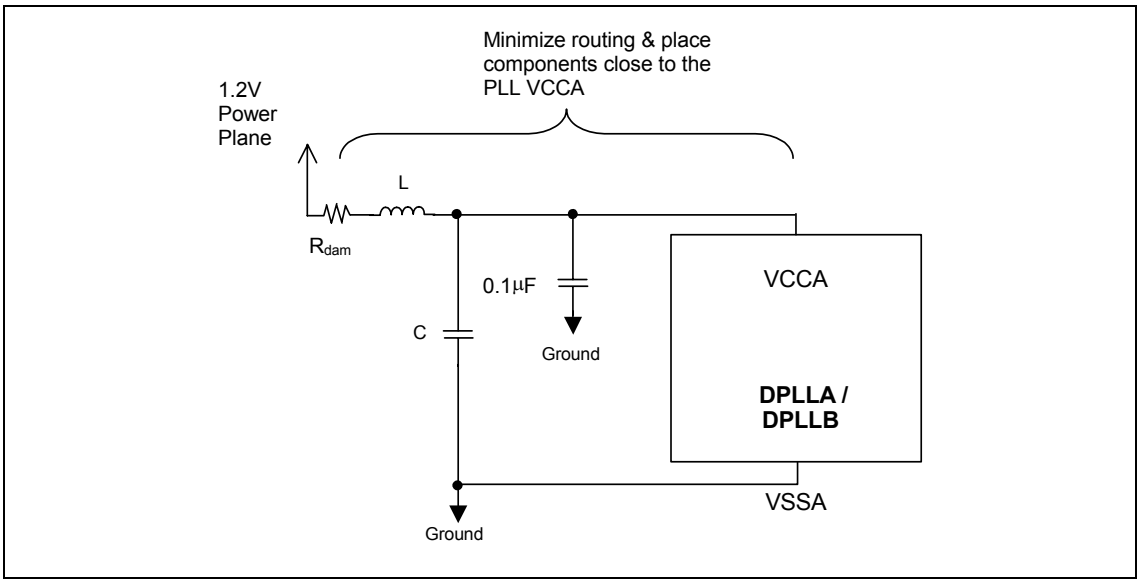
A 0.1-µF decoupling capacitor is necessary for both the HPLL and CPLL. The decoupling capacitor should connect between the analog power pin and the board ground plane with the capacitor placed as close to the VCCA balls as possible. If possible route the capacitor to the DPLL_VSSA ball before terminating to ground. The capacitor should have low parasitic. A 0.1-µF capacitor with a maximum ESR rating of 10 mΩ and an ESL rating of 0.9 nH is recommended.

7.1.2. Display PLLs

The display PLLs (DPLLA and DPLLB) on the Intel 830 Chipset family GMCH-M require better supply filtering compared to the HPLL and CPLL because noise that exits on the analog power rail of the display PLLs may result in distorted or jittered displays. A low-pass LC filter is recommended for the display PLL analog power so that dot clock jitter is minimized.

The following figure shows a block diagram showing the recommended topology of the filter along with the recommended high-frequency de-coupling capacitor. The display PLL analog power rail (VCCDA) is connected to the 1.2-V board power plane through an LC filter.

Figure 28. Recommended LC Filter and Decoupling Capacitor for Each DPLL



The resistance from the inductor to the board 1.2-V power plane represents the total resistance from the board power plane to the filter capacitor. This resistance, which can be a physical resistor, routing/via resistance, parasitic resistance of the inductor or combinations of these, acts as a damping resistance for the filter and effects the response of the filter. A physical resistor may not be needed depending on the resistance of the inductor and the routing/via resistance. The maximum current flowing into the analog power rail for the PLL is approximately 30 mA.

The filter capacitance should be chosen with as low of an ESR (equivalent series resistance) and ESL (equivalent series inductance) as possible in order to achieve the best filter performance. The parasitics of the LC filter capacitor can alter the characteristics of the filter significantly and even cause the filter to be ineffective at the frequencies of interest.

7.1.3. Recommended Routing/Component Placement

- The filter capacitance should be placed as close to the VCCA ball as possible.
- The VSSA ball should via down to the board ground plane. (If possible route VSSA to the decoupling capacitor C as show in Figure 28.)
- The filter inductor should be placed in close proximity to the filter capacitor.
- If a discrete resistor is used for the LC filter, the resistor should be placed between the 1.2-V board power plane connection and the filter inductor.

7.1.4. Recommended DPLL LC Filter Components

Capacitor Description: 100 µF +/- 20%, 16VDC, ESR=0.14 Ω @ 100 kHz, ESL=2.5 nH

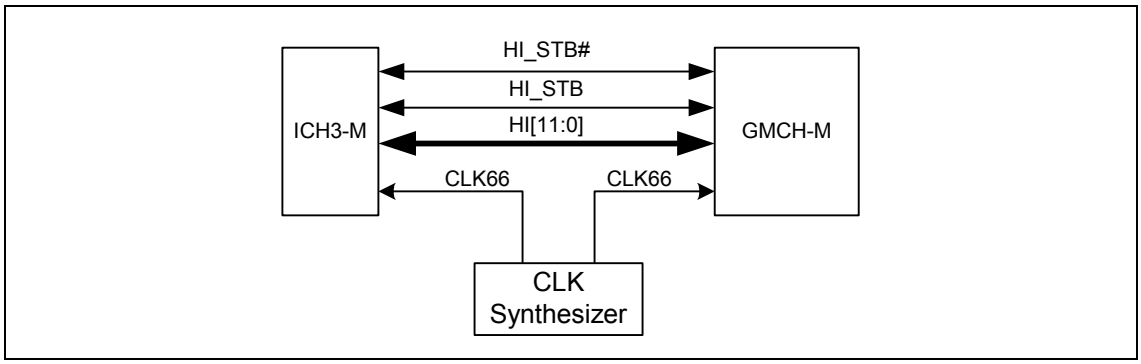
Inductor Description: 100 nH +/- 10%, 250 mA, Max dc resistance = 0.26 Ω, size=0805, magnetically shielded

Resistor Description: 1.0 Ω, 1%, 1/16 W, SMT metal film

8. Hub Interface

The Intel 830 Chipset family GMCH-M and ICH3-M ballout assignments have been optimized to simplify the hub interface routing between these devices. Intel recommends that the hub interface signals be routed directly from the GMCH-M to ICH3-M with all signals referenced to VSS. Layer transition should be kept to a minimum. If a layer change is required, use only two Vias per net and keep all data signals and associated strobe signals on the same layer. The hub interface signals are broken into two groups: data signals (HL) and strobe signals (HL_STB).

Figure 29. 8-Bit Hub Interface Routing Example



8.1. Hub Interface Routing Guidelines

This section documents the routing guidelines for the 8-bit hub interface. This hub interface connects the ICH3-M and the GMCH-M. The hub interface uses a compensation signal to adjust buffer characteristics to the specific board characteristic. The hub interface requires Resistive Compensation (RCOMP).

The trace impedance must equal 55 Ω ± 15%.

Table 29. Hub Interface RCOMP Resistor Values

Component	Trace Impedance	HICOMP Resistor Value	HICOMP Resistor Tied to
ICH3-M	55 Ω ± 15%	36.5 Ω ± 1%	VSS
GMCH-M	55 Ω ± 15%	55 Ω ± 1%	VSS

8.2. Hub Interface Data Signals

These data signal traces should be routed 5-mils wide with 10 mils trace spacing (5 on 10) and 15-mils spacing from other signals. In order to break out of the Intel 830 Chipset family GMCH-M and ICH3-M packages, the hub interface data signals can be routed 5-mils wide with 5-mil spacing. The signal must be separated to 5-mil width with 10-mil spacing within 300 mils from the package.

The maximum hub interface data signal trace length is 6 inches. Each data signal must be matched within ± 200 mils of the HL_STB differential pair. There is no explicit matching requirement between the individual data signals.

8.3. Hub Interface Strobe Signals

The Hub Interface strobe signals should be routed as a differential pair, 5 mils wide with 10 mils trace spacing (5 on 10) and 15 mils spacing from other signals. This strobe pair should have a minimum of 15-mils spacing from any other adjacent signals. The maximum length for the strobe signals is 6 inches. Each strobe signal must be the same length, and each data signal must be matched to within ± 200 mils of the strobe signals.

8.4. HUBREF/HIREF Generation/Distribution

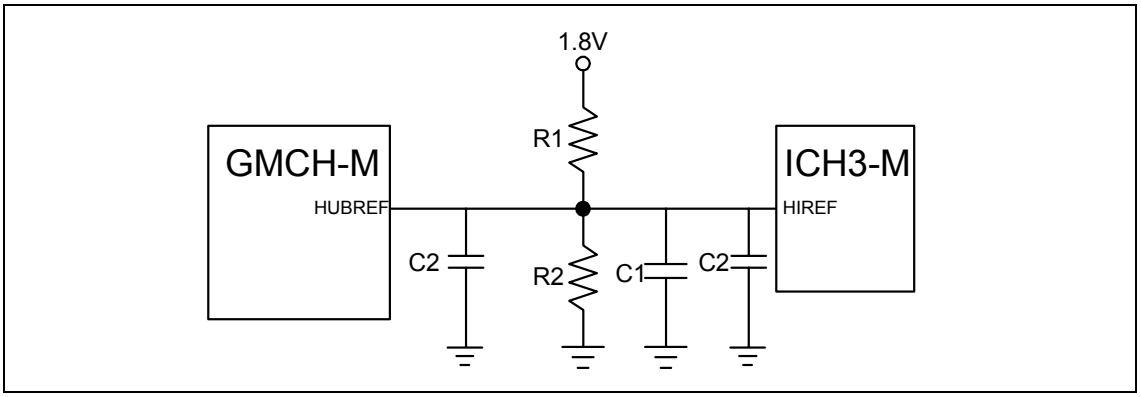
HUBREF(HIREF pin on ICH3-M) is the hub interface reference voltage. Depending on the buffer mode, the HUBREF voltage requirement must be set appropriately for proper operation. See the table below for the HUBREF voltage specifications and the associated resistor recommendations for the voltage divider circuit.

Table 30. Hub Interface HUBREF Generation Circuit Specifications

HUBREF Voltage Specification (V)	Recommended Resistor Values for the HUBREF Divider Circuit (Ω)
1/2 VCC1_8 ± 2%	R1 = R2 = 301 ± 1%

The single HUBREF divider should be located in the middle of the bus (three inches from GMCH-M and ICH3-M) between the GMCH-M and ICH3-M. If the single HUBREF divider is located more than four inches away, locally generated Hub Interface reference dividers should be used instead. The reference voltage generated by a single HUBREF divider should be bypassed to ground at each component with a 0.01-µF capacitor located close to the component HUBREF pin. If the reference voltage is generated locally, the bypass capacitor needs to be close to the component HUBREF pin.

Table 31. 8-Bit Hub Interface With Single Reference Divider Circuit



8.5. Hub Interface Decoupling Guidelines

To improve I/O power delivery, use two 0.1-µF capacitors per each component (i.e. the ICH3-M and GMCH-M). These capacitors should be placed within 150 mils from each package, adjacent to the rows that contain the Hub Interface. If the layout allows, wide metal fingers running on the VSS side of the board should connect the VCC1_8 side of the capacitors to the VCC1_8 power pins. Similarly, if layout allows, metal fingers running on the VCC1_8 side of the board should connect the groundside of the capacitors to the VSS power pins.

9. I/O Subsystem

9.1. IDE Interface

This section contains guidelines for connecting and routing the ICH3-M IDE interface. The ICH3-M has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement, and signal termination for both IDE channels. The ICH3-M has integrated the series resistors that have been typically required on the IDE data signals (PDD[15:0] and SDD[15:0]) running to the two ATA connectors. While it is not anticipated that additional series termination resistors will be required, OEMs should verify motherboard signal integrity through simulation. Additional external 0-Ω resistors can be incorporated into the design to address possible noise issues on the motherboard. The additional resistor layout increases flexibility by offering stuffing options at a later date.

The IDE interface can be routed with 5-mil traces on 7-mil spaces, and must be less than 8 inches long (from ICH3-M to IDE connector). Additionally, the shortest IDE signal (on a given IDE channel) must be less than 0.5 inch shorter than the longest IDE signal (on that channel). See Table 32 below for reference.

Table 32. IDE Signals

Signal	Max length (inch)	Width (mils)	Space (mils)	Relative Mismatch max length (mils)	Relative To	Space with other signals (mils)
Signal Group#ide1 IDE_PDD[15:0] IDE_SDD[15:0] IDE_PDA2 IDE_PDCS3# IDE_PATADET IDE_SATADET IDE_SEC_RST# IDE_PRI_RST# IDE_PDA0 IDE_PDA1 IDE_PDCS1# IDE_PDDACK# IDE_PDDREQ IDE_PDIOW# IDE_SDA0 IDE_SDA1 IDE_SDA2	8	5	7	± 250	Shortest and longest IDE signal in same channel	8

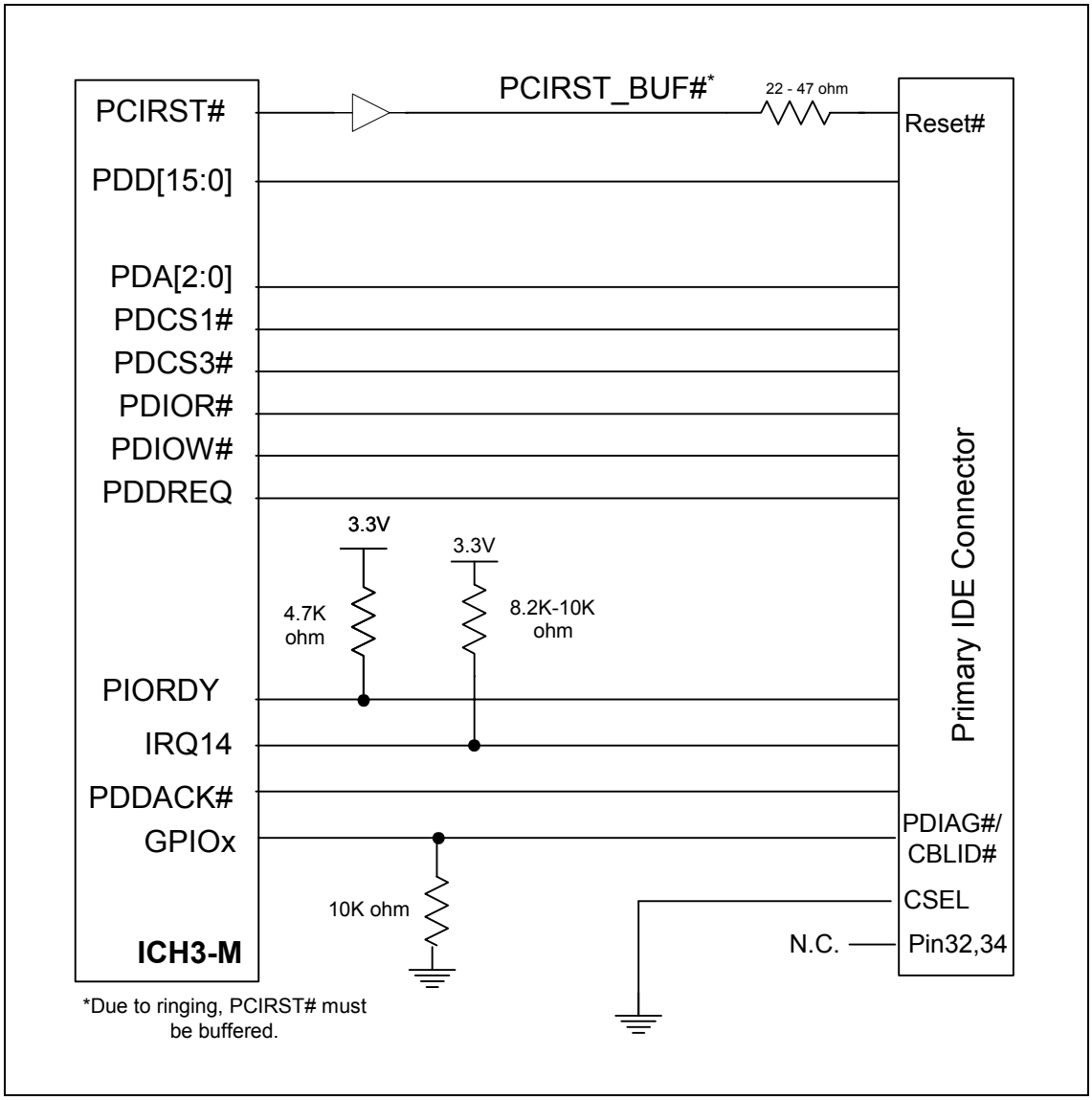
IDE_SDCS1# IDE_SDCS3# IDE_SDDACK# IDE_SDDREQ IDE_SDIOW#						
Signal Group#ide2 IDE_PIORDY IDE_PDIOR# IDE_SIORDY IDE_SDIOR#	8	5	7	± 5	IDE_PIORDY with IDE_PDIOR# And IDE_SIORDY with IDE_SDIOR#	8
Other signals INT_IRQ1 IDE_PDACTIVE# INT_IRQ15 IDE_SDACTIVE#						

9.1.1. Cable Requirements

- Length of cable: Each IDE cable must be equal to or less than 18 inches.
- Capacitance: Less than 30 pF.
- Placement: A maximum of 6 inches between drive connectors on the cable. If a single drive is placed on the cable it should be placed at the end of the cable. If a second drive is placed on the same cable, it should be placed on the next closest connector to the end of the cable (6 inches away from the end of the cable).
- Grounding: Provide a direct low impedance chassis path between the motherboard ground and hard disk drives.
- ICH3-M Placement: The ICH3-M must be placed equal to or less than 8 inches from the ATA connector(s).

9.1.2. Primary IDE Connector Requirements

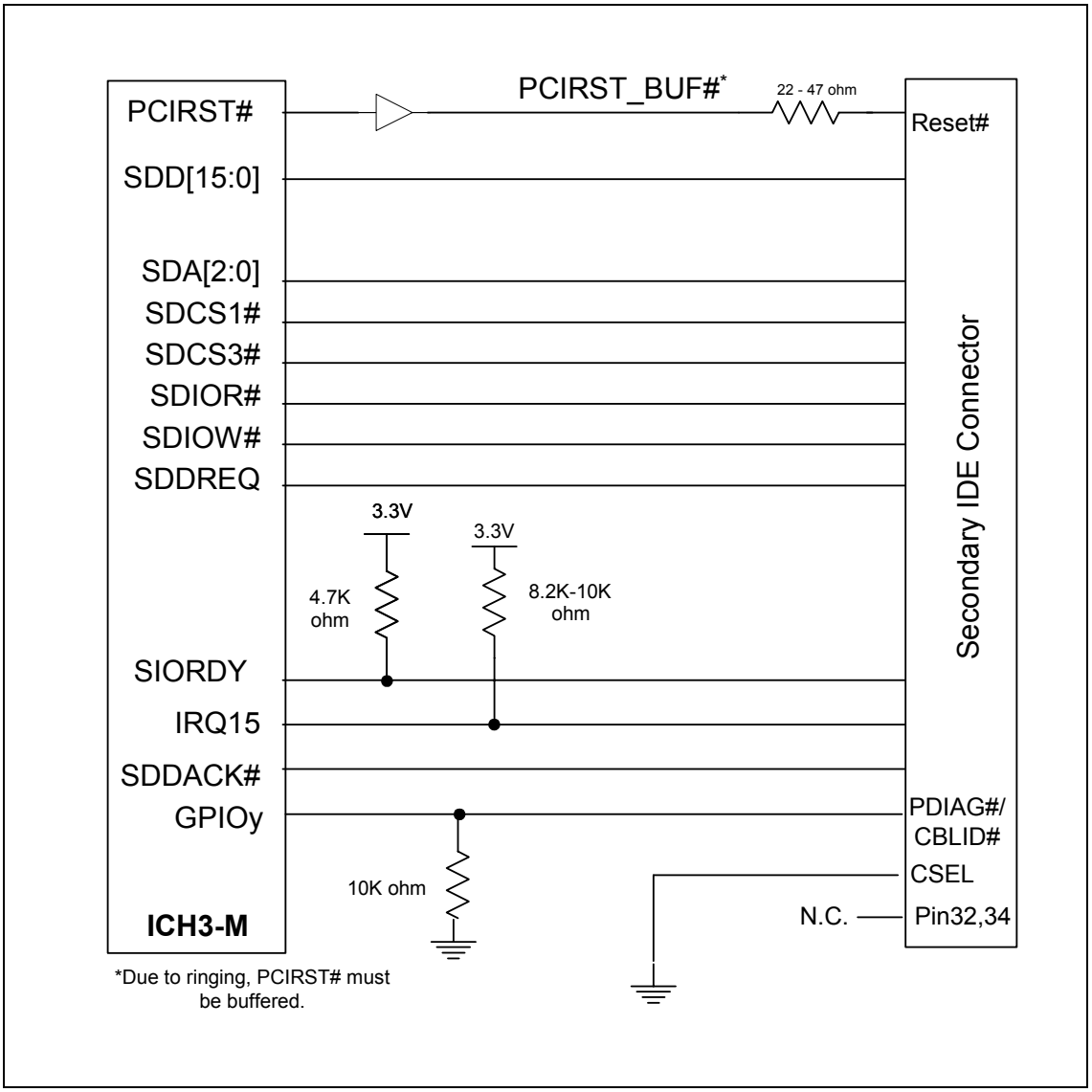
Figure 30. Connection Requirements for Primary IDE Connector



- 22-Ω to 47-Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
- An 8.2-kΩ to 10-kΩ pull-up resistor is required on IRQ14 and IRQ15 to Vcc3_3.
- A 4.7-kΩ pull-up resistor to Vcc3_3 is required on PIORDY and SIORDY.
- Series resistors can be placed on the control and data line to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.
- A 10-kΩ pull-down resistor to ground is required on the PDIAG#/CBLID# signal. This is to prevent the GPI pin from floating if a device is not present on the Primary IDE interface.

9.1.3. Secondary IDE Connector Requirements

Figure 31. Connection Requirements for Secondary IDE Connector



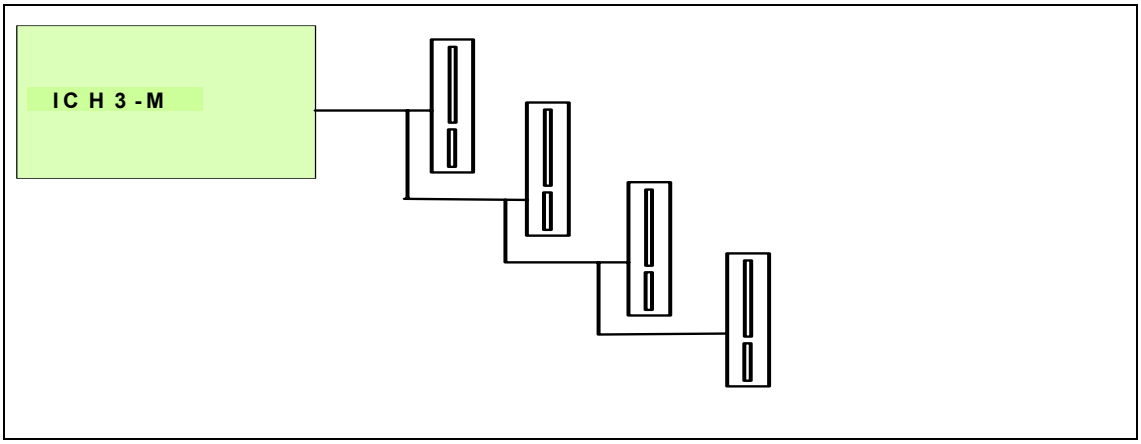
- 22-Ω to 47-Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
- An 8.2-kΩ to 10-kΩ pull-up resistor is required on IRQ14 and IRQ15 to Vcc3_3.
- A 4.7 kΩ pull-up resistor to Vcc3_3 is required on PIORDY and SIORDY.
- Series resistors can be placed on the control and data line to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.
- A 10-kΩ pull-down resistor to ground is on the PDIAG#/CBLID# signal is now required on the Secondary Connector. This change is to prevent the GPI pin from floating if a device is not present on the Secondary IDE interface.

9.2. PCI

The ICH3-M provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification Revision 2.2*. The implementation is optimized for high-performance data streaming when the ICH3-M is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, refer to the *PCI Local Bus Specification Revision 2.2*.

The ICH3-M supports six PCI Bus masters (excluding the ICH3-M), by providing six REQ#/GNT# pairs. In addition, the ICH3-M supports two PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

Figure 32. PCI Bus Layout Example

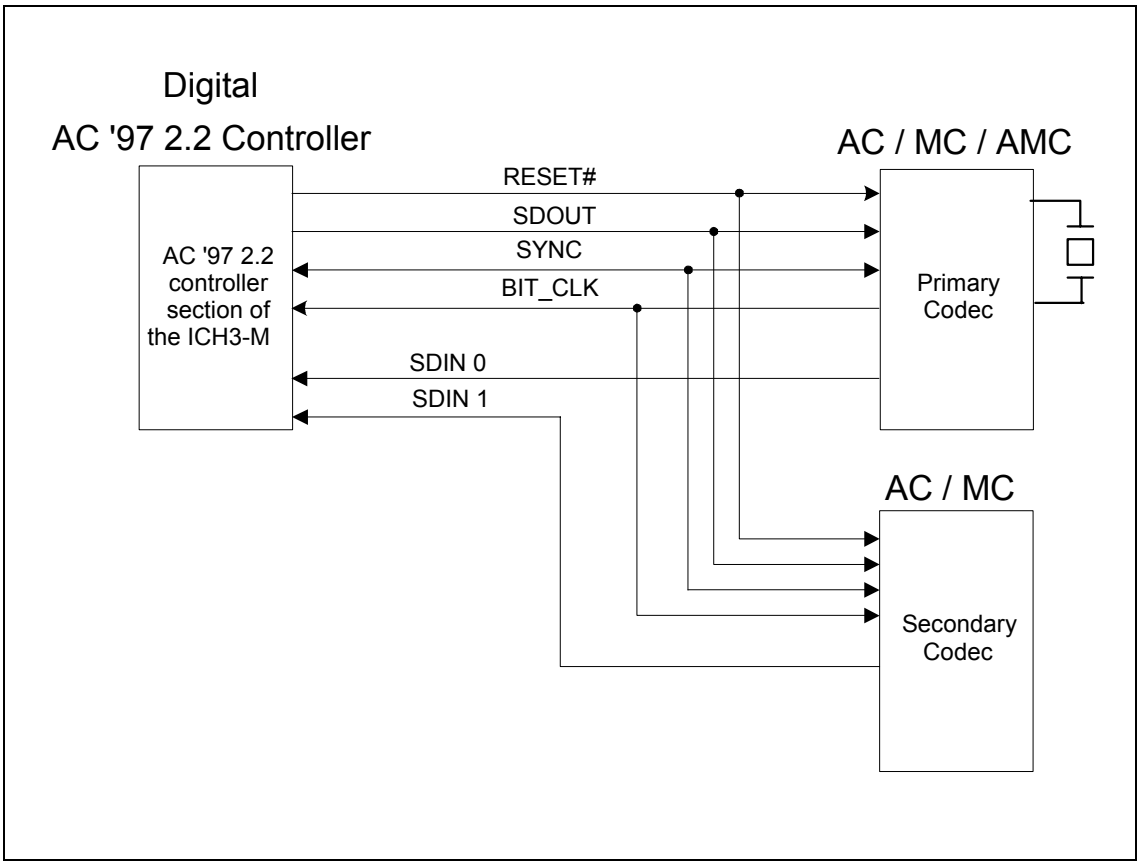


9.3. AC'97

The ICH3-M implements an AC'97 2.2 compliant digital controller. Attached AC'97 codecs on the ICH3-M AC-link may be AC'97 2.1 or 2.2 compliant. Please contact your codec IHV for information on AC'97 compliant products. Please refer to Section 1.1 for the AC'97 specifications.

The AC-link is a bi-directional, serial PCM digital stream. It handles multiple input and output data streams, as well as control register accesses, employing a time division multiplexed (TDM) scheme. The AC-link architecture provides for data transfer through individual frames transmitted in a serial fashion. Each frame is divided into 12 outgoing and 12 incoming data streams, or slots. The architecture of the ICH3-M AC-link allows a maximum of two codecs to be connected. The following figure shows a two-codec topology of the AC-link for the ICH3-M.

Figure 33. ICH3-M AC'97 – Codec Connection



9.3.1. Four-Layer Layout Example

Using the assumed 4-layer stack-up, the AC'97 interface can be routed using 5-mil traces with 5-mil space between the traces. Maximum length between ICH3 to CODEC/CNR is 14 inches in a "T" topology. Trace impedance should be $Z_0 = 60\ \Omega \pm 15\%$.

Clocking is provided from the primary codec on the link via BITCLK, and is derived from a 24.576-MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. BITCLK is a 12.288-MHz clock driven by the primary codec to the digital controller (ICH3-M), and any other codec present. That clock is used as the timebase for latching and driving data.

The ICH3-M supports wake on ring from S1M-S5 via the AC'97 link. The codec asserts AC_SDINn to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

The ICH3-M has weak pull-downs / pull-ups that are only enabled when the AC-Link Shut Off bit in the ICH3-M is set or if both function 5 and function 6 of device 31 are disabled (hidden). This will keep the link from floating when the AC-link is off, or there are no codecs present.

If the Shut-off bit is not set, or if neither function 5 nor function 6 of device 31 are disabled (hidden), it implies that there is a codec on the link. Therefore, BITCLK and AC_SDOUT will be driven by the codec and ICH3-M respectively. However, AC_SDIN0 and AC_SDIN1 may not be driven. If the link is enabled, the assumption can be made that there is at least one codec.

9.3.2. AC'97 Audio Codec Detect Circuit and Configuration Options

The following provides general circuits to implement a number of different codec configurations. Please refer to Intel's White Paper Recommendations for ICHx/AC'97 Audio (Motherboard and Communication and Network Riser) for Intel's recommended codec configurations (available at the URL given in Section 1.1).

To support more than two channels of audio output, the ICH3-M allows for a configuration where two audio codecs work concurrently to provide surround capabilities. To maintain data-on-demand capabilities, the ICH3-M AC'97 controller, when configured for 4 or 6 channels, will wait for all the appropriate slot request bits to be set before sending data in the SDATA_OUT slots. This allows for simple FIFO synchronization of the attached codecs. It is assumed that both codecs will be programmed to the same sample rate, and that the codecs have identical (or at least compatible) FIFO depth requirements. It is recommended that the codecs be provided by the same vendor, upon the certification of their interoperability in an audio channel configuration.

9.3.3. Valid Codec Configurations

Table 33. Codec Configurations

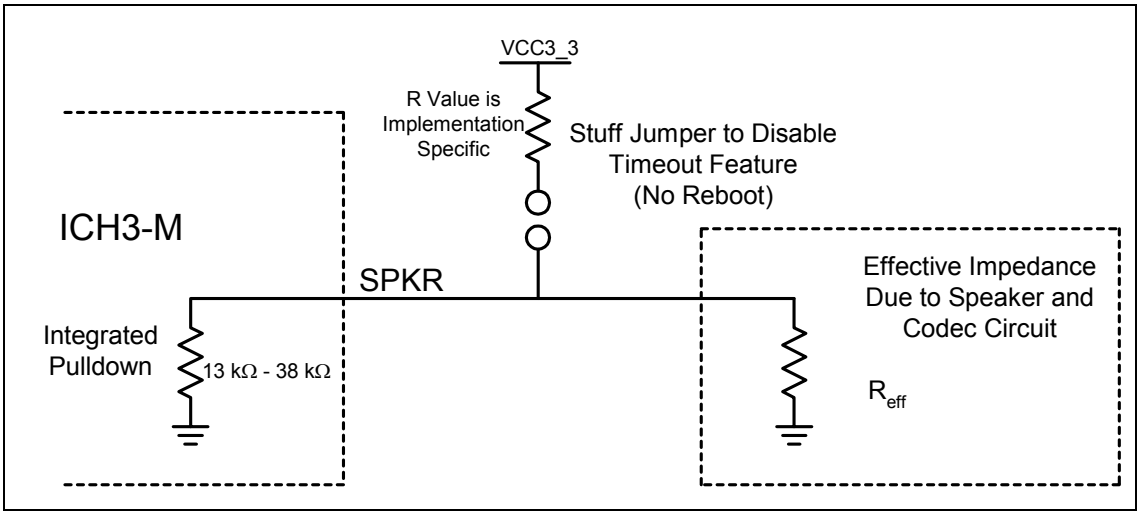
Valid Codec Configurations
AC(Primary)
MC(Primary)
AMC(Primary)
AC(Primary) + MC(Secondary)
AC(Primary) + AC(Secondary)
AC(Primary) + AMC(Secondary)

Invalid Codec Configurations
MC(Primary) + X(any other type of codec)
AMC(Primary) + AMC(Secondary)
AMC(Primary) + MC(Secondary)

9.3.4. SPKR Pin Consideration

SPKR is used as both the output signal to the system speaker and as a functional strap. The strap function enables or disables the "TCO Timer Reboot function" based on the state of the SPKR pin on the rising edge of PWROK. When enabled, the ICH3-M sends an SMI# to the Processor upon a TCO timer timeout. The status of this strap is readable via the NO_REBOOT bit (bit 1, D31: F0, Offset D4h). The SPKR signal has a weak integrated pull-down resistor (the resistor is only enabled during boot/reset). Therefore, its default state is a logical zero or set to reboot. To disable the feature, a jumper can be populated to pull the signal line high (see the following figure). The value of the pull-up must be such that the voltage divider output caused by the pull-up, the effective pull-down (R_{eff}), and the ICH3-M's integrated pull-down resistor will be read as logic high (0.5 Vcc3_3 to Vcc3_3 + 0.5 V).

Figure 34. Example Speaker Circuit



9.3.5. AC'97 Routing

To ensure the maximum performance of the codec, proper component placement and routing techniques are required. These techniques include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground planes, from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio section. Contact your vendor for device-specific recommendations.

The basic recommendations are as follows:

- Special consideration must be given for the ground return paths for the analog signals.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.
- Partition the board with all analog components grouped together in one area and all digital components in another.
- Separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inches wide.
- Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.
- Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (0.25 inches to 0.5 inches wide) where the analog/isolated ground plane connects to the main ground plane. The split between planes must be a minimum of 0.05 inches wide.
- Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main motherboard ground. That is, no signal should cross the split/gap between the ground planes, which would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.
- Analog power and signal traces should be routed over the analog ground plane.

- Digital power and signal traces should be routed over the digital ground plane.
- Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance.
- All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors can be used for DC voltages and the power supply path, where the voltage coefficient, temperature coefficient, and noise are not factors.
- Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane.
- Locate the crystal or oscillator close to the codec.

Clocking is provided from the primary codec on the link via BITCLK, and it is derived from a 24.576-MHz crystal or oscillator. Refer to the primary codec vendor for the crystal or oscillator requirements. BITCLK is a 12.288-MHz clock driven by the primary codec to the digital controller (ICH3-M) and by any other codec present. The clock is used as the time base for latching and driving data.

9.3.6. Motherboard Implementation

The following design considerations are provided for the implementation of an ICH3-M platform using AC'97. These design guidelines have been developed to ensure maximum flexibility for board designers, while reducing the risk of board-related issues. These recommendations are not the only implementation or a complete checklist, but they are based on the ICH3-M platform.

- Components such as FET switches, buffers or logic states should not be implemented on the AC-link signals, except for AC_RST#. Doing so would potentially interfere with timing margins and signal integrity.
- The ICH3-M supports wake-on-ring from S1M-S5 states via the AC'97 link. The codec asserts AC_SDIN*n* to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec. If no codec is attached to the link, internal pull-downs will prevent the inputs from floating, so external resistors are not required.

PC_BEEP should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

9.4. USB Guidelines and Recommendations

9.4.1. General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design. These guidelines will help to minimize signal quality and EMI problems. The USB validation efforts focused on a four-layer motherboard where the first layer is a signal layer, the second plane is power, the third plane is ground and the fourth is a signal layer. This will result in placing most of the routing on the fourth plane closest to the ground plane, and allowing a higher component density on the first plane. For mobile motherboards with different stackup, all USB signals should be ground referenced when using the appropriate layer for routing.

- Place the ICH3-M and major components on the unrouted board first. With minimum trace lengths, route high-speed clock, periodic signals and USB differential pairs first. Maintain maximum possible distance between high-speed clocks/periodic signals to USB differential pairs and any connector leaving the PCB (i.e., I/O connectors, control and signal headers, or power connectors).
- USB signals should be ground referenced.
- Route USB signals using a minimum of vias and corners. This reduces reflections and impedance changes.
- When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities.
- Do not route USB traces under crystals, oscillators, clock synthesizers, magnetic devices or IC's that use and/or duplicate clocks.
- Stubs on USB signals should be avoided, as stubs have an effect on signal quality. If a stub is necessary in the design, no stub should be greater than 200 mils.
- Route all traces over continuous planes, (VCC or GND) with no interruptions. Avoid crossing over anti-etch if at all possible. This increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces.
- Keep USB signals clear of the core logic set. High current transients are produced during internal state transitions, which can be very difficult to filter out.
- Keep traces at least 50 mils away from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires and also helps prevent free radiation of the signal from the edge of the PCB.

9.4.2. USB Trace Separation

Use the following separation guidelines.

- Recommended trace width and separation is 5-mil trace with a 6-mil space (90-Ω differential impedance).

Note: The goal is to have a 90-Ω differential impedance and the spacing may need to be different depending on the stackup.

- Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90 ohms differential impedance.
- Use at a minimum 20-mil spacing between USB signal pair and other traces on the PCB. This helps to prevent crosstalk. If possible, keep clock and PCI traces at least 50 mils from the USB differential pairs.
- Minimize the length of high-speed clock and periodic signal traces that run parallel to USB signal lines to minimize crosstalk.

9.4.3. USB Trace Length Matching

Use the following trace length matching guidelines.

- USB signal pair traces should be trace length matched.

Table 34. USB Signals

Signal	Max length (inch)	Width (mils)	Space (mils)	Mismatch length (mils)	Relative To	Space with other signals (mils)	Notes
USB Signals Group USB_PN0 to USB_PN5 USB_PP0 to USB_PP5	10 (min 3.5)	4	6	±75	Signal differential pair	20	Clock and PCI should be 50 mils away from USB signals (min)

9.4.4. Plane Splits, Voids, and Cut-Outs (Anti-Etch)

The following guidelines apply to the use of plane splits voids and cut-outs.

9.4.4.1. VCC Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Use the following guidelines for the VCC plane.

- Traces should not cross anti-etch, for it greatly increases the return path for those signal traces. This can be true of USB signals, high-speed clocks, and signal traces as well as slower signal traces that might be coupling to them.
- Avoid routing of USB signals 50-mil of any anti-etch to avoid coupling to the next split or radiating from the edge of the PCB.

9.4.4.2. GND Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Use the following guideline for the GND plane.

- Avoid anti-etch on the GND plane.

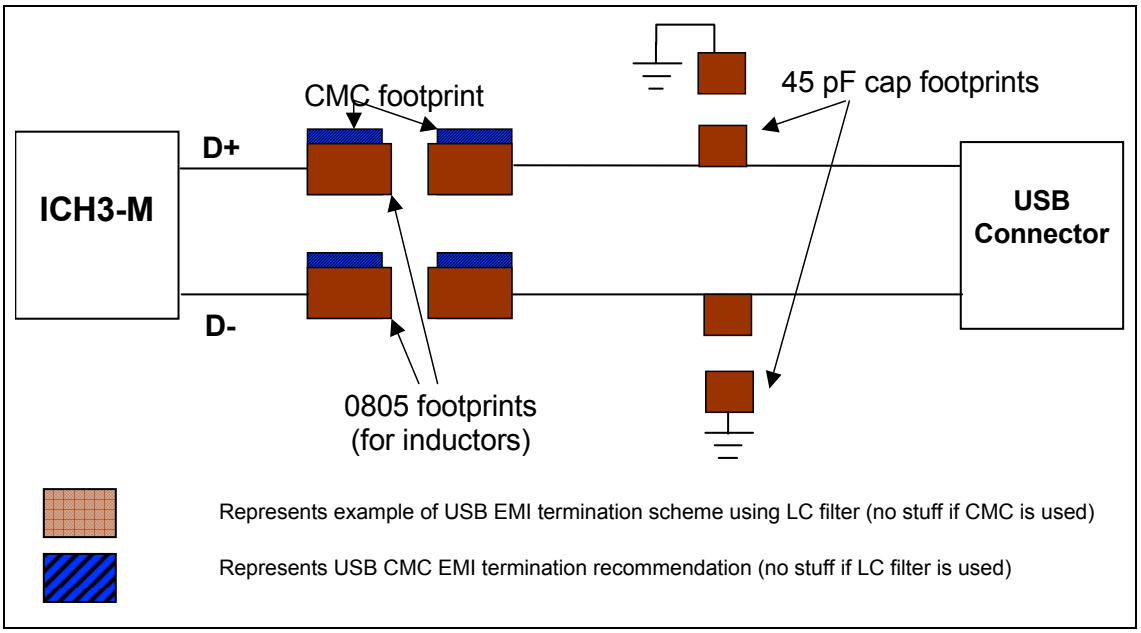
9.4.5. EMI Considerations

9.4.5.1. USB Board Design Flexibility

The ICH3-M platform may have been designed to support a common-mode choke footprint for EMI solutions. In this configuration, the board may use a common-mode choke (CMC) for USB EMI, although the cost of the part may yield this as an undesirable solution. To offer maximum flexibility and potential cost savings, a board may be designed to support with the CMC or USB signals with the existing (cheaper) EMI solutions. Figure 35 provides an example layout utilizing a dual-footprint option. If the CMC is used, it is critical that the capacitor footprints are left unpopulated, as capacitors would break USB signal integrity.

The figure below shows an example of a board utilizing a 0805 inductor and a 45-pF capacitor for each data line for its USB EMI solution. By modifying the footprint of the 0805 inductor to overlap with the CMC's footprint, the board can support either the inductors or a CMC.

Figure 35. USB EMI Dual Footprint Example



9.5. IOAPIC (I/O Advanced Programmable Interrupt Controller)

Note: The Intel 830 Chipset family platform does not support IOAPIC when C2/C3/C4 states are enabled.

Mobile Systems not using the IOAPIC should disable IOAPIC functionality through the system BIOS.

9.5.1. IOAPIC Disabling Options

9.5.1.1. Recommended Implementation

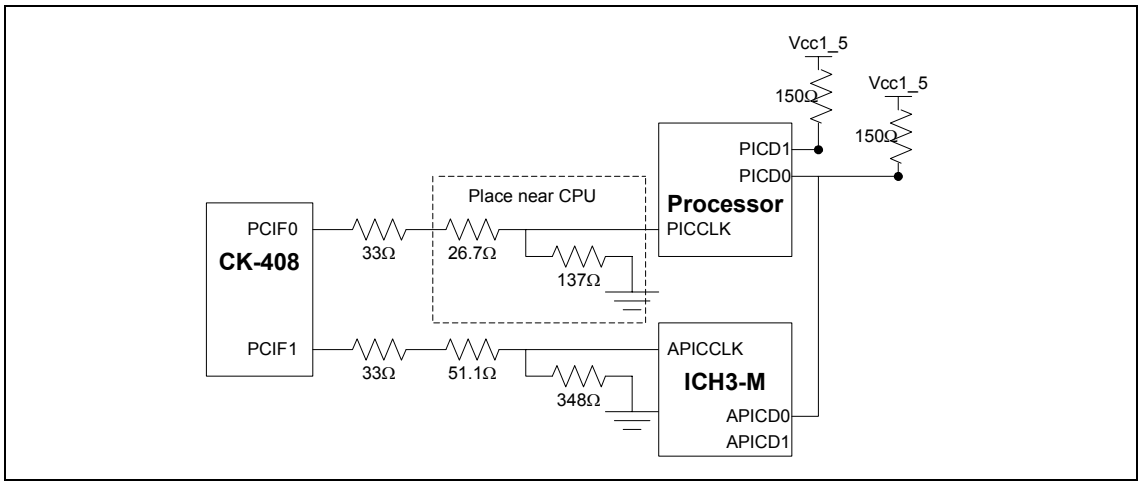
Intel recommends that IOAPIC be disabled in software and the hardware configuration on the board is implemented as shown in Figure 36.

To disable IOAPIC in BIOS:

1. ICH3-M: D31:F0; Offset: D0-D3h; bit 8 (0=disable);
2. Mobile Intel Pentium III Processor-M/Mobile Intel Celeron Processor MSR 1Bh bit 11 (0 = disable)

This has been validated on the Intel CRB and allows flexibility of future IOAPIC use. Software can be used to turn off PICCLK if desired.

Figure 36. Recommended IOAPIC Disable Topology



9.5.1.2. Minimum Requirements for Disabling IOAPIC

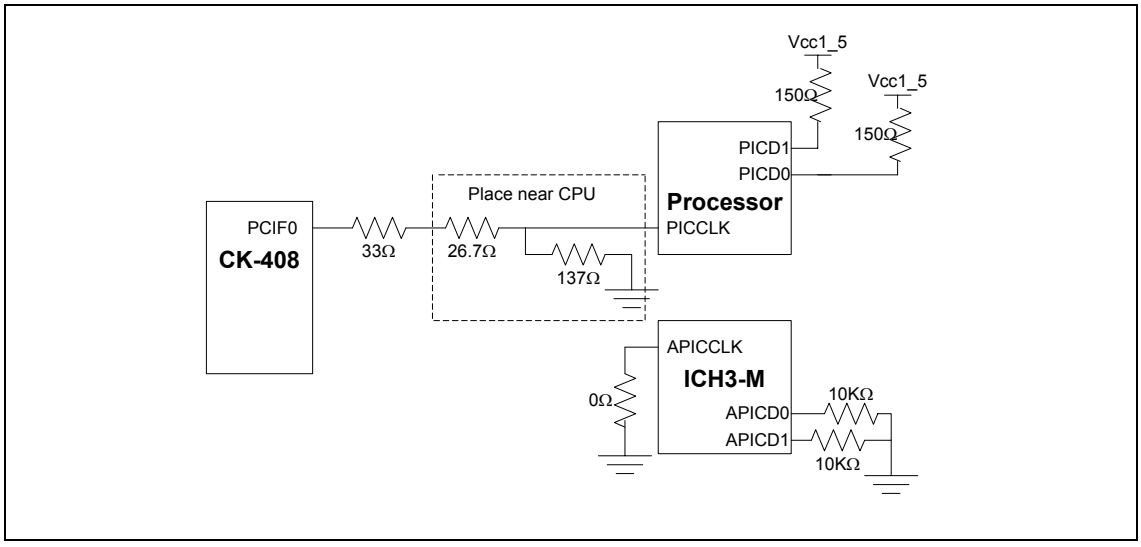
If the above recommended requirements as described in Section 9.5.1.1 cannot be met on a particular platform design, then the following minimum set of guidelines should be implemented.

Intel recommends that IOAPIC be disabled in software and the hardware configuration on the board is implemented as shown in the Figure 37.

To disable IOAPIC in BIOS:

1. ICH3-M: D31:F0; Offset: D0-D3h; bit 8 (0=disable);
2. Mobile Intel Pentium III Processor-M/ Mobile Intel Celeron Processor: MSR 1Bh bit 11 (0 = disable)

Figure 37. Minimum IOAPIC Disable Topology



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9.5.2. PIRQ Routing Example

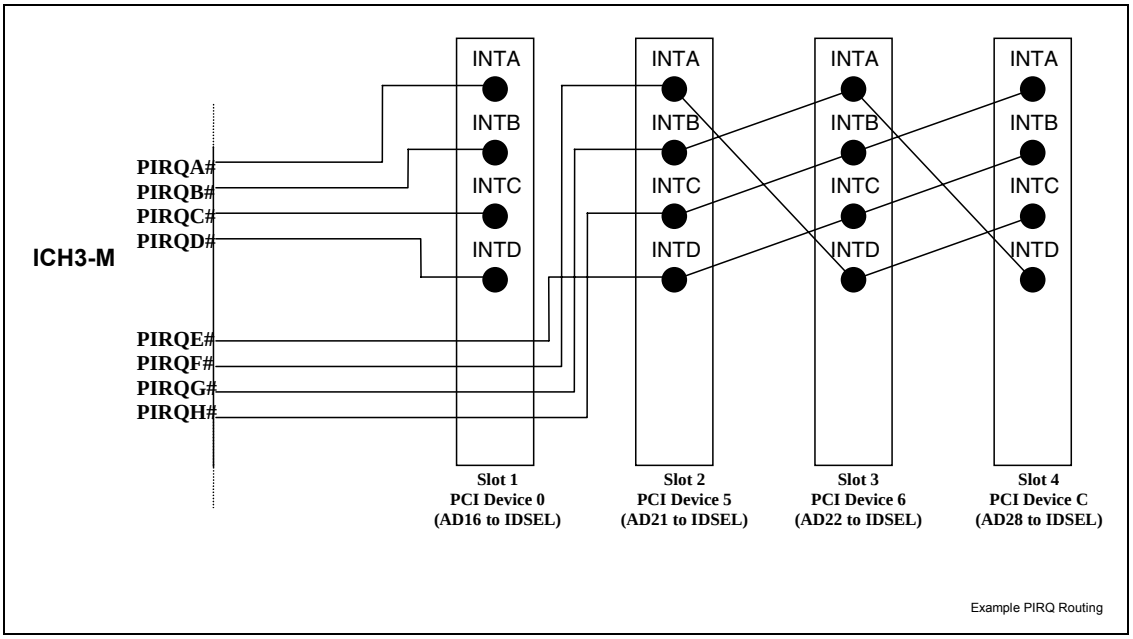
PCI interrupt request signals E-H are new to the ICH3-M. These signals have been added to lower the latency caused by having multiple devices on one Interrupt line. With these new signals, a system can be designed to minimize sharing of PCI interrupt request lines. The following table shows how the ICH3-M uses the PCI IRQ when the IOAPIC is active.

Table 35. IOAPIC Interrupt Inputs 16 Through 23 Usage

Number	IOAPIC INTIN PIN	Function in ICH3-M using the PCI IRQ in IOAPIC
1	IOAPIC INTIN PIN 16 (PIRQA)	USB Controller #1
2	IOAPIC INTIN PIN 17 (PIRQB)	AC'97 Audio and Modem; option for SMBus
3	IOAPIC INTIN PIN 18 (PIRQC)	USB Controller #3; Native IDE
4	IOAPIC INTIN PIN 19 (PIRQD)	USB Controller #2
5	IOAPIC INTIN PIN 20 (PIRQE)	Internal LAN; option for SCI, TCO
6	IOAPIC INTIN PIN 21 (PIRQF)	Option for SCI, TCO
7	IOAPIC INTIN PIN 22 (PIRQG)	Option for SCI, TCO
8	IOAPIC INTIN PIN 23 (PIRQH)	Option for SCI, TCO

Due to different system configurations, IRQ line routing to the PCI slots ("swizzling") should be made to minimize the sharing of interrupts between both internal ICH3 functions and PCI functions. The figure below shows an example of IRQ line routing to the PCI slots (note: it is not necessarily an optimal routing scheme; an optimal scheme depends on individual system PCI IRQ usage).

Figure 38. Example PIRQ Routing



The above figure is an example. It is up to the board designer to route these signals in a way that will prove the most efficient for their particular system. A PCI slot can be routed to share interrupts with any of the ICH3-M's internal device/functions (but at a higher latency cost).

9.6. SMBus 2.0/SMLink Interface

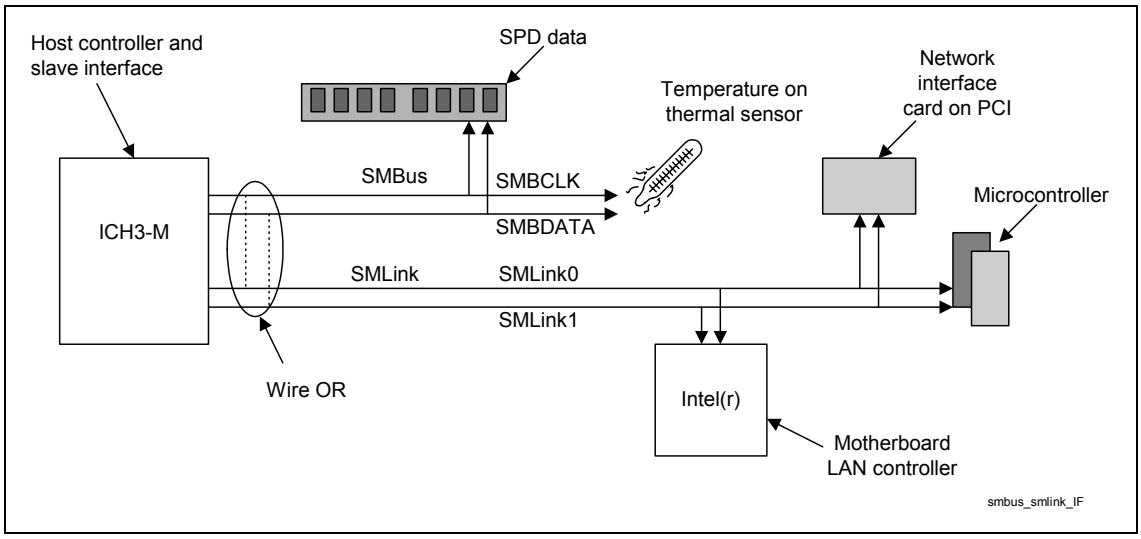
The SMBus interface on the ICH3-M is the same as that on the ICH2-M. It uses two signals SMBCLK and SMBDATA to send and receive data from components residing on the bus. These signals are used exclusively by the SMBus Host Controller. The SMBus Host Controller resides inside the ICH3-M. If the SMBus is used only for the RAMBUS* SPD EEPROMs (one on each RIMM*), both signals should be pulled up with a 4.7-kΩ resistor to 3.3 V.

The ICH3-M incorporates an SMLink interface supporting AOL*, AOL2* and a slave functionality. It uses two signals SMLINK[1:0]. SMLINK[0] corresponds to an SMBus clock signal and SMLINK[1] corresponds to an SMBus data signal. These signals are part of the SMB Slave Interface.

For Alert on LAN* (AOL*) functionality, the ICH3-M transmits heartbeat and event messages over the interface. When using the Intel 82562EM Platform LAN Connect Component, the ICH3-M's integrated LAN Controller will claim the SMLink heartbeat and event messages and send them out over the network. An external, AOL2*-enabled LAN Controller (i.e., Intel 82550) will connect to the SMLink signals to receive heartbeat and event messages, as well as access the ICH3-M SMBus Slave Interface. The slave interface function allows an external microcontroller to perform various functions. For example, the slave write interface can reset or wake a system, generate SMI# or interrupts, and send a message. The slave read interface can read the system power state, read the watchdog timer status, and read system status bits.

Both the SMBus Host Controller and the SMBus Slave Interface obey the SMBus 1.0 protocol, so the two interfaces can be externally wire-OR'd together to allow an external management ASIC (such as Intel® 82550) to access targets on the SMBus as well as the ICH3-M Slave interface. Additionally, the ICH3-M supports slave functionality, including the Host Notify protocol, on the SMLink pins. Therefore, in order to be fully compliant with the SMBus 2.0 specification (which requires the Host Notify cycle), the SMLink and SMBus signals **must** be tied together externally. This is done by connecting SMLink[0] to SMBCLK and SMLink[1] to SMBDATA.

Figure 39. SMBUS 2.0/SMLink Interface



NOTE: Intel does not support external access of the ICH3-M's Integrated LAN Controller via the SMLink interface. Also, Intel does not support access of the ICH3-M's SMBus Slave Interface by the ICH3-M's SMBus Host Controller.

9.6.1. SMBus Architecture and Design Considerations

9.6.1.1. SMBus Design Considerations

There are several possibilities for designing a SMBus using the ICH3-M. Designs can be grouped into three major categories based on the power supply source for the SMBus microcontrollers. This includes two unified designs, where either Vcc_Core or Vcc_Suspend powers all devices, and a mixed design where some devices are powered by each of the two supplies.

Primary considerations in choosing a design are based on the following:

- Are there devices that must run in STR?
- Amount of Vcc_Suspend current available, i.e. minimizing load of Vcc_Suspend.

9.6.1.2. General Design Issues/Notes

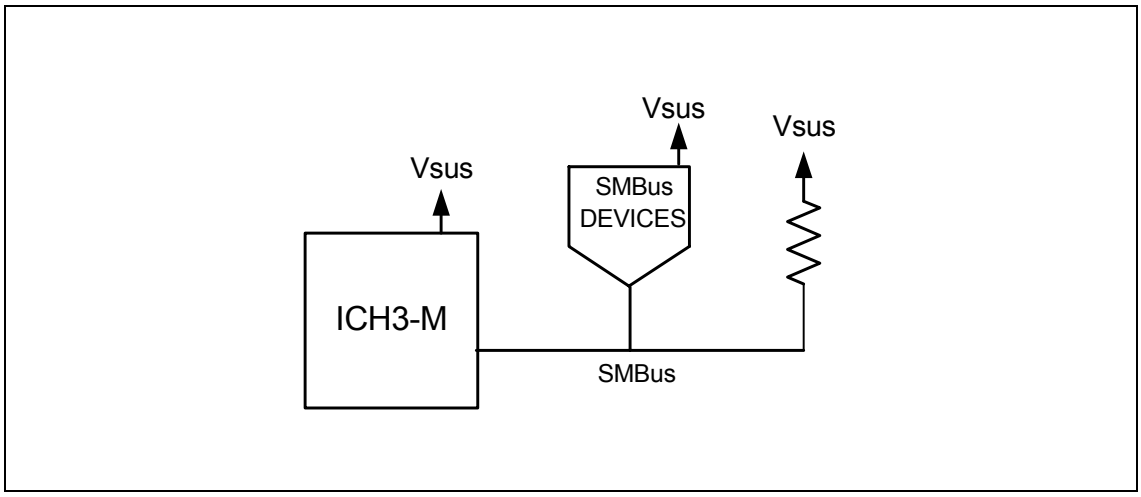
Regardless of the architecture used, there are some general considerations. See below.

- The pull-up resistor size for the SMBus data and clock signals is dependent on the number of devices present on the bus. A typical value is 8.2 KΩ. This should prevent the SMBus signals from floating, which could cause leakage in the ICH3-M and other devices.
- SDRAM SO-DIMMs have their SPD device powered by the same power plane as that used for the DRAM array. Thus in a system where STR is supported, the SPD device must be powered by VCC_Suspend. In a system not supporting STR, this SO-DIMM can be powered by the core supply.
- RIMM* memory modules have a separate power source from the DRDRAM* array for the SPD device. If this SPD device needs to operate in STR, then it should be connected to the VCC_Suspend supply.
- The ICH3-M does not run SMBus cycles while in STR.
- SMBus devices that can operate in STR must be powered by the Vcc_Suspend supply.

9.6.1.3. The Unified Vcc_ Suspend Architecture

In this design all SMBus devices are powered by the Vcc_Suspend supply. Consideration must be made to provide enough Vcc_Suspend current while in STR.

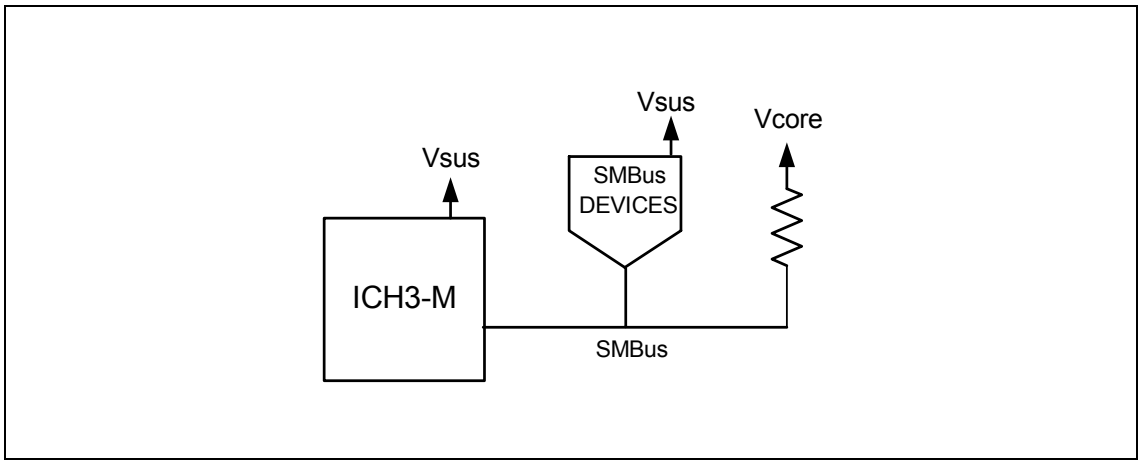
Figure 40. Unified Vcc_Suspend Architecture



9.6.1.4. The Unified Vcc_Core Architecture

In this design, all SMBUS devices are powered by the Vcc_Core supply. This architecture allows none of the devices to operate in STR, but minimizes the load on Vcc_Suspend.

Figure 41. Unified Vcc_Core Architecture



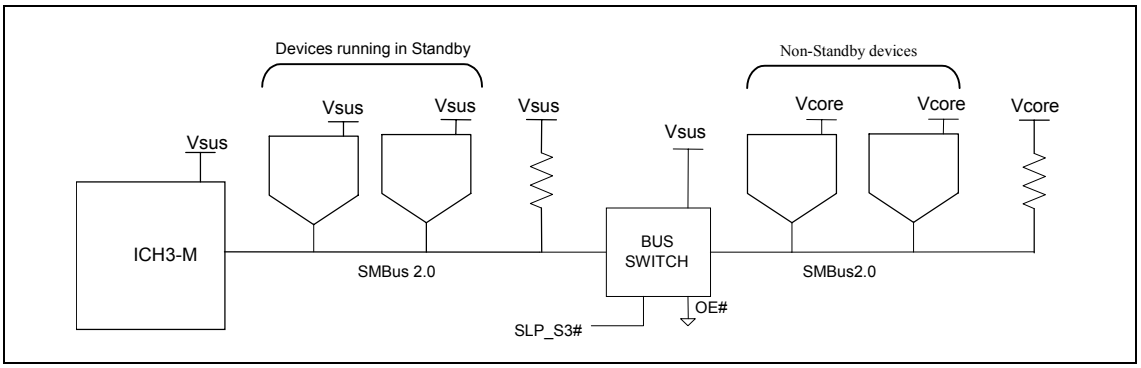
NOTES:

1. The SMBus device needs to be back-drive safe while its supply (Vcore) is off and Vcc_Suspend is still powered.
2. In suspended modes where Vcc_Core is OFF & Vcc_Suspend is on, the Vcc_Core node will be very near ground. In this case the input leakage of the ICH3-M will be approximately 10 µA.

9.6.1.5. Mixed Architecture

This design allows for SMBus devices to communicate while in STR, yet minimizes Vcc_Suspend leakage by keeping non-essential devices on the core supply. This is accomplished by the use of a “bus switch” to isolate the devices powered by the core and suspend supplies.

Figure 42. Mixed Vcc_Suspend/Vcc_Core Architecture



Added Considerations for Mixed Architecture:

- The bus switch must be powered by Vcc_Suspend
- If there are 5-V SMBus devices used, then an added level translator must be used to separate those devices driving 5 V from those driving 3-V signal levels.
- Devices that are powered by the Vcc_Suspend well must not drive into other devices that are powered off. This is accomplished with the “bus switch”.

9.7. FWH

The following provides general guidelines for compatibility and design recommendations for supporting the FWH device. The majority of the changes will be incorporated in the BIOS. For assistance, please consult your local Intel Field Application Engineers.

9.7.1. FWH Decoupling

A 0.1-µF capacitor should be placed between the Vcc supply pins and the Vss ground pins to decouple high frequency noise, which may affect the programmability of the device. Additionally, a 4.7-µF capacitor should be placed between the Vcc supply pins and the Vss ground pins to decouple low frequency noise. The capacitors should be placed no further than 390 mils from the Vcc supply pins.

9.7.2. In Circuit FWH Programming

All cycles destined for the FWH will appear on PCI. The ICH3-M hub interface to PCI Bridge will put all CPU boot cycles out on PCI (before sending them out on the FWH interface). If the ICH3-M is set for subtractive decode, these boot cycles can be accepted by a positive decode agent on the PCI bus. This enables the ability to boot from of a PCI card that positively decodes these memory cycles (in order to boot off a PCI card, it is necessary to keep the ICH3-M in subtractive decode mode). If a PCI boot card is inserted and the ICH3-M is programmed for positive decode, there will be two devices positively decoding the same cycle. In systems with the 82380AB (ISA bridge), it is also necessary to keep the NOGO signal asserted when booting from a PCI ROM. Note that it is not possible to boot off a ROM behind the 82380AB. Once you have booted from the PCI card, you could potentially program the FWH in circuit and program the ICH3-M CMOS.

9.8. FWH Signaling Voltage Compatibility

Depending on the V_CPU_IO of the Processor and the manufacturer of the FWH, there may be signaling voltage compatibility issues with the ICH3-M. The range of acceptable V_CPU_IO for the ICH3-M is 1.2 V to 2.5 V. If the processor core voltage is not within this range, translation logic will be required on the processor side before even considering the FWH.

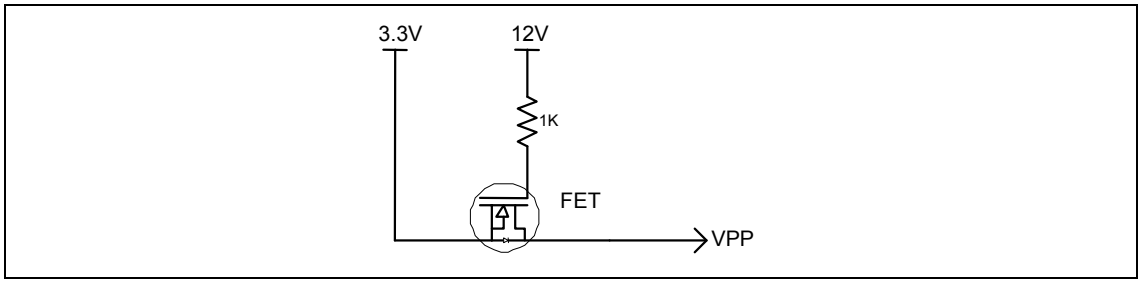
Furthermore, the FWH INIT signal trip points need to be considered because they are NOT consistent among different FWH manufacturers. The INIT signal is active low. Therefore, the inactive state of the ICH3-M INIT signal needs to be at a value slightly higher than the V_{IH} min FWH INIT pin specification. The ICH3-M inactive state of this signal is governed by the formula V_CPU_IO - 0.13 V. Therefore, if the V_CPU_IO of the processor is 1.5 V and the V_{IH} min spec of the FWH INIT input signal is 1.35 V, there would be no compatibility issue because 1.5 V - 0.13 V = 1.37 V which is greater than the 1.35 V minimum of the FWH. If the V_{IH} min of the FWH was 1.4 V, then there would be an incompatibility and logic translation would need to be used. Note that these examples do not take into account noise that may be encountered on INIT. Care must be taken to ensure that the VIM min specification is met with ample noise margin.

9.8.1. FWH Vpp Design Guidelines

The Vpp pin on the FWH is used for programming the flash cells. The FWH supports Vpp of 3.3 V or 12 V. If Vpp is 12 V the flash cells will program about 50% faster than at 3.3 V. However, the FWH only supports 12-V Vpp for 80 hours. The 12 V Vpp would be useful in a programmer environment, which is typically an event that occurs very infrequently (much less than 80 hours). The VPP pin MUST be tied to 3.3 V on the motherboard.

In some instances, it is desirable to program the FWH during assembly with the device soldered down on the board. In order to decrease programming time it becomes necessary to apply 12 V to the V_{PP} pin. The following circuit will allow testers to put 12 V on the V_{PP} pin while keeping this voltage separated from the 3.3- V plane to which the rest of the power pins are connected. This circuit also allows the board to operate with 3.3 V on this pin during normal operation.

Figure 43. FWH VPP Isolation Circuitry



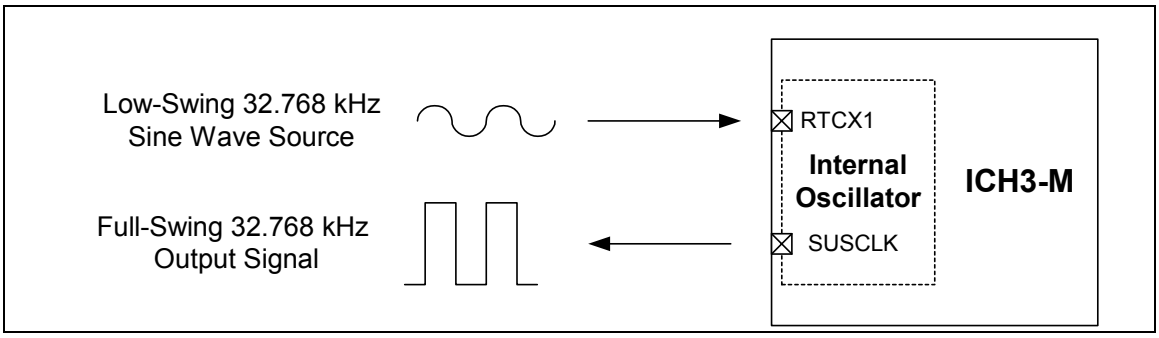
9.9. RTC

The ICH3-M contains a real time clock (RTC) with 256 bytes of battery backed SRAM. The internal RTC module provides two key functions: keeping date and time and storing system data in its RAM when the system is powered down.

The ICH3-M uses a crystal circuit to generate a low-swing 32 kHz input sine wave. This input is amplified and driven back to the crystal circuit via the RTCX2 signal. Internal to the ICH3-M, the

RTCX1 signal is amplified to drive internal logic as well as generate a free running full swing clock output for system use. This output ball of the ICH3-M is called SUSCLK. See Figure 44 below.

Figure 44. RTCX1 and SUSCLK Relationship in ICH3-M



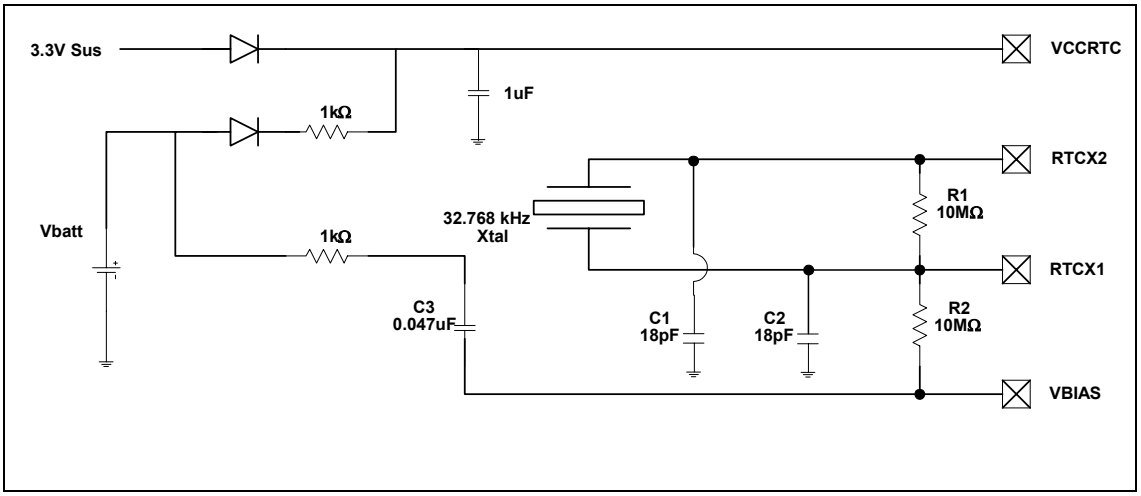
For further information on the RTC, please consult the "Intel ICH Family Real Time Clock (RTC) Accuracy and Considerations under Test Conditions, Application Note AP- 728 r1.0" which can be found at: http://developer.intel.com/design/chipsets/applnots/292276.htm

9.9.1. RTC Crystal

This section will present the recommended hookup for the RTC circuit for the ICH3-M.

The ICH3-M RTC module requires an external oscillating source of 32.768 kHz connected on the RTCX1 and RTCX2 balls. The following figure documents the external circuitry that comprises the oscillator of the ICH3-M RTC.

Figure 45. External Circuitry for the ICH3-M RTC

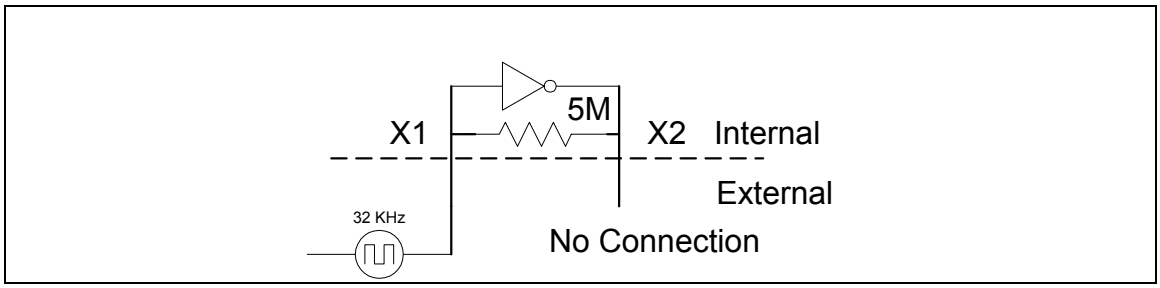


NOTES:

1. The exact capacitor value needs to be based on what the crystal maker recommends. (Typical values for C2 and C3 are 18 pF for a crystal load of 12 pF)
2. V_{CCRTC}: Power for RTC Well
3. RTCX2: Feedback for the external crystal
4. RTCX1: Input to the internal oscillator
5. V_{BIAS}: RTC BIAS Voltage – This ball is used to provide a reference voltage, and this DC voltage sets a current, which is mirrored throughout the oscillator and buffer circuitry.

Note: Even if the ICH3 internal RTC is not used, it is still necessary to supply clock inputs to X1 and X2 of the ICH3 because other signals are gated off that clock in suspend modes. However, in this case, the frequency (32.768 kHz) of the clock inputs is not critical; a lower-cost crystal can be used or a single clock input can be driven into X1 with X2 left as no connect; Figure 46 illustrates this. **This is not a validated configuration with ICH3-M.**

Figure 46. RTC Connections When Not Using Internal RTC



9.9.2. External Capacitors

To maintain the RTC accuracy, the external capacitor C3 needs to be 0.047 µF, and the capacitor values (C1 and C2) should be chosen to provide the manufacturer's specified load capacitance (Cload) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. The following equation can be used to choose the external capacitance values (C2 and C3):

Equation 2. RTC External Capacitor Equation

$$C_{load} = [(C_1 + C_{in1} + C_{trace1})*(C_2 + C_{in2} + C_{trace2})]/[(C_1 + C_{in1} + C_{trace1} + C_2 + C_{in2} + C_{trace2})] + C_{parasitic}$$

Where:

- C_{load} = Crystal's load capacitance. This value can be obtained from crystal's specification.
- C_{in1}, C_{in2} = input capacitances at RTCX1, RTCX2 balls of the ICH3-M. These values can be obtained in the ICH3-M Datasheet.
- C_{trace1}, C_{trace2} = Trace length capacitances measured from crystal terminals to RTCX1, RTCX2 balls. These values depend on the characteristics of board material, the width of signal traces and the length of the traces. Typical value is approximately equal to:
  C_{trace} = trace length * 2 pF / inch (dependent upon board characteristics)
- $C_{parasitic}$ = Crystal's parasitic capacitance. This capacitance is created by the existence of two electrode plates and the dielectric constant of the crystal blank inside the crystal part. Refer to the crystal's specification to obtain this value.

Ideally, C_1, C_2 can be chosen such that $C_1 = C_2$. Using the equation of C_{load} above, the value of C_1, C_2 can be calculated to give the best accuracy (closest to 32.768 kHz) of the RTC circuit at room temperature. However, C_2 can be chosen such that $C_2 > C_1$. Then C_1 can be trimmed to obtain 32.768 kHz.

In certain conditions, both C_1, C_2 values can be shifted away from the **theoretical values** (calculated values from the above equation) to obtain the closest oscillation frequency to 32.768 kHz. When C_1, C_2 value are smaller then the theoretical values, the RTC oscillation frequency will be higher.

The following example will illustrates the use of the practical values C_1, C_2 in the case that theoretical values can not guarantee the accuracy of the RTC in low temperature condition:

Example 1:

According to a required 12-pF load capacitance of a typical crystal that is used with the ICH3, the calculated values of $C_1 = C_2$ is 10 pF at room temperature (25^0 C) to yield an 32.768-kHz oscillation.

At 0^0 C the frequency stability of crystal gives –23 ppm (assumed that the circuit has 0 ppm at 25^0 C). This makes the RTC circuit oscillate at 32.767246 kHz instead of 32.768 kHz.

If the values of C_1 , C_2 are chosen to be 6.8 pF instead of 10 pF. This will make the RTC oscillate at higher frequency at room temperature (+23 ppm) but this configuration of C_1 / C_2 makes the circuit oscillate closer to 32.768 kHz at 0^0 C. The 6.8 pF value of C1 and C2 is the **practical value**.

Note that the temperature dependency of crystal frequency is parabolic relationship (ppm / degree square). The effect of changing crystal's frequency when operating at 0°C (25°C below room temperature) is the same when operating at 50°C (25°C above room temperature).

9.9.3. RTC Layout Considerations

- Keep the RTC lead lengths as short as possible; around ¼ inch is sufficient.
- Minimize the capacitance between Xin and Xout in the routing.
- Put a ground plane under the XTAL components.
- Don't route switching signals under the external components (unless on the other side of the board).
- The oscillator Vcc should be clean; use a filter, such as an RC lowpass, or a ferrite inductor.
- Trace signal coupling must be reduced by avoiding routing of adjacent PCI signals close to RTCX1 and RTCX2, VBIAS.

9.9.4. RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH3-M is not powered by the system.

Example batteries are: Duracell* 2032, 2025, or 2016 (or equivalent), which can give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 3 µA, the battery life will be at least:

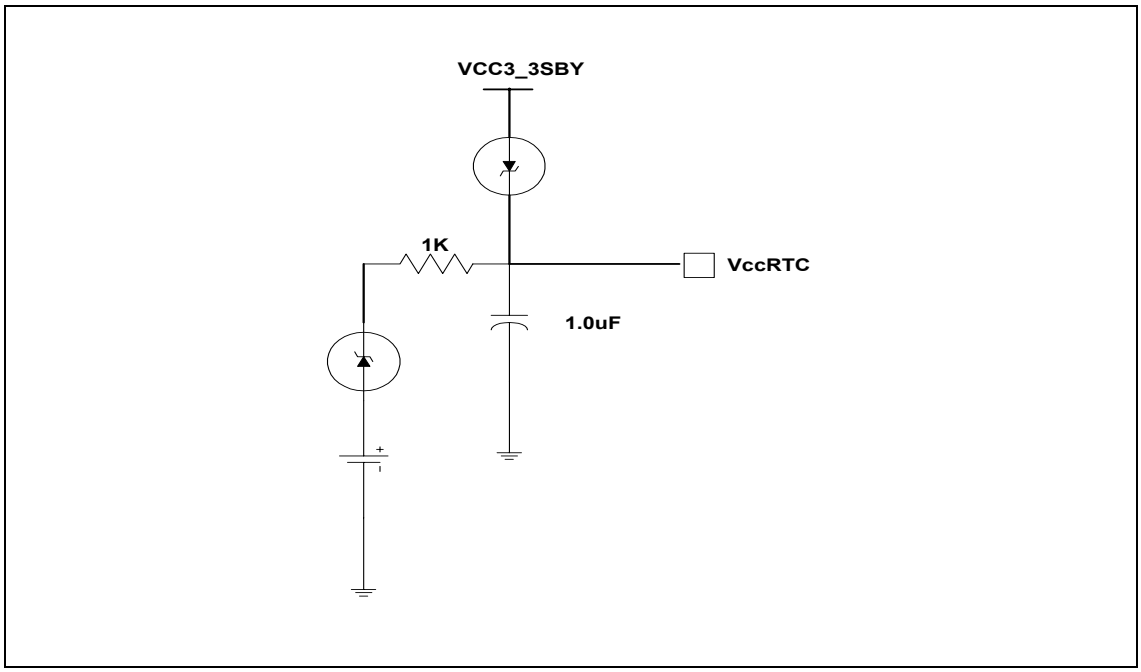
Equation 3. RTC External Battery Life Equation

170,000 uAh / 3 uA = 56,666 h = 6.4 years

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. The battery voltage of the RTC must be greater than 2 V at all time to ensure the accuracy of the RTC clock. The battery must be connected to the ICH3-M via an isolation schottky diode circuit. The schottky diode circuit allows the ICH3-M RTC-well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this,

the diodes are set to be reverse biased when the system power is not available. The following figure is an example of a diode circuit that is used.

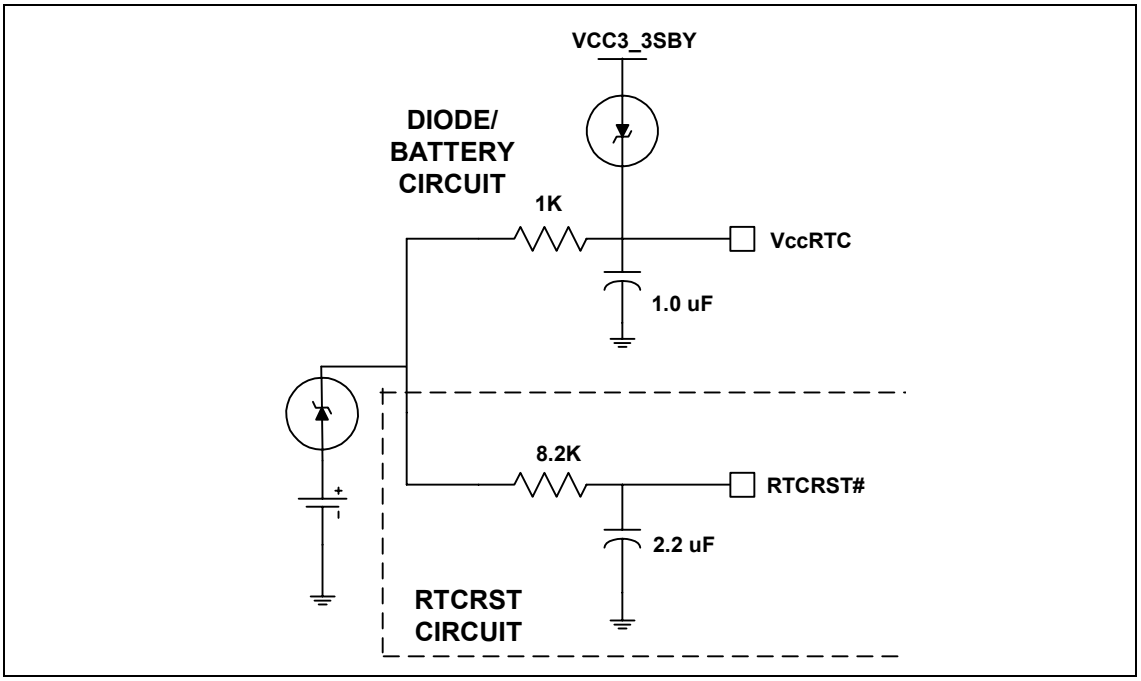
Figure 47. A Diode Circuit to Connect RTC External Battery



A standby power supply should be used in a Mobile system to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and thereby the RTC accuracy.

9.9.5. RTC External RTCRST# Circuit

Figure 48. RTCRST# External Circuit for the ICH3-M RTC



The ICH3-M RTC requires some additional external circuitry. The RTCRST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTCRST# and the RTC battery (Vbat) were selected to create an RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 10-20 ms. When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1, and remains set until software clears it. As a result of this, when the system boots, the BIOS knows that the RTC battery has been removed.

This RTCRST# circuit is combined with the diode circuit which allows the RTC well to be powered by the battery when the system power is not available. The previous figure is an example of this circuitry that is used in conjunction with the external diode circuit.

9.9.6. RTC Routing Guidelines

- All RTC OSC signals (RTCX1, RTCX2, VBIAS) should all be routed with trace lengths of less than 1 inch, the shorter the better.
- Minimize the capacitance between RTCX1 and RTCX2 in the routing (optimal would be a ground line between them).
- Put a ground plane under all of the external RTC circuitry.
- Don’t route any switching signals under the external components (unless on the other side of the ground plane).

9.9.7. VBIAS DC Voltage and Noise Measurements

VBIAS is a DC voltage level that is necessary for biasing the RTC oscillator circuit. This DC voltage level is filtered out from the RTC oscillation signal by the RC Network of R2 and C3 (see Figure 45) therefore it is self-adjusted voltage. Board designers should not manually bias the voltage level on VBIAS. Checking VBIAS level is used for testing purposes only to determine the right bias condition of the RTC circuit.

VBIAS should be at least 200-mV DC. The RC network of R2 and C3 will filter out most of AC signal that exist on this ball, however, the noise on this ball should be kept minimal in order to guarantee the stability of the RTC oscillation.

Probing VBIAS requires the same technique as probing the RTCX1, RTCX2 signals (using Op-Amp). Consult your Intel Field Application Engineer for further details on measuring techniques.

Note that VBIAS is also very sensitive to environmental conditions.

9.9.8. SUSCLK

SUSCLK is a square waveform signal output from the RTC oscillation circuit. Depending on the quality of the oscillation signal on RTCX1 (largest voltage swing), SUSCLK duty cycle can be between 30-70%. If the SUSCLK duty cycle is beyond 30-70% range, it indicates a poor oscillation signal on RTCX1 and RTCX2.

SUSCLK can be probed directly using normal probe (50Ω input impedance probe) and it is an appropriated signal to check the RTC frequency to determine the accuracy of the ICH3-M's RTC Clock (contact your Intel Field Application Engineer for more details).

9.9.9. RTC-Well Input Strap Requirements

All RTC-well inputs (RSMRST#, RTCRST#, INTRUDER# and PWROK) must be either pulled up to V_{CC}RTC or pulled down to ground while in G3 state. RTCRST# when configured meets this requirement. RSMRST# should have a weak external pull-down (8-22 kΩ) to ground and INTRUDER# should have a weak external pull-up to V_{CC}RTC. This will prevent these nodes from floating in G3, and correspondingly will prevent I_{CC}RTC leakage that can cause excessive coin-cell drain. The PWROK input signal should also be configured with an external weak pull-down of 8-22 kΩ .The details are shown in the figure below. The arrows in bold indicate the leakage paths if appropriate pull-ups and pull-downs are not present.

9.10. Internal LAN Layout Guidelines

The ICH3-M provides several options for integrated LAN capability. The platform supports several components depending on the target market. These guidelines use 82562ET to refer to both the Intel 82562ET and the Intel 82562EM. The 82562EM is specified in those cases where there is a difference.

Table 36. Integrated LAN Capability

Platform LAN Connect component	Connection	Features
Intel 82562EM	Advanced 10/100 Ethernet	AOL* & Ethernet 10/100 Connection

Intel 82562ET	10/100 Ethernet	Ethernet 10/100 Connection
Intel 82562EH	1 Mb HomePNA* LAN	1 Mb HomePNA* connection

Intel developed a dual footprint for the Intel 82562ET and Intel 82562EH to minimize the required number of board builds. A single layout with the specified dual footprint will allow the OEM to install the appropriate Platform LAN Connect component to meet the market need.

Figure 49. ICH3-M/LAN Connect Section (Dual Footprint Option)

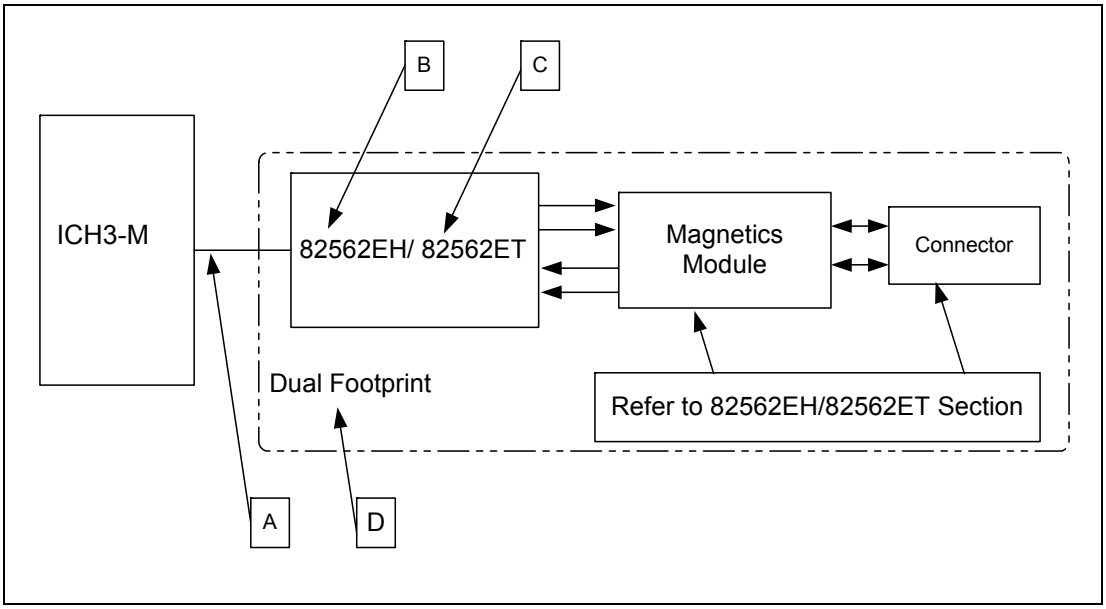


Table 37. LAN Design Guide Section Reference

Layout Section	Figure 13-22 Reference	Design Guide Section
ICH3-M – LAN Interconnect	A	ICH3-M – LAN Interconnect Guidelines
General Routing Guidelines	B,C,D	
82562EH	B	
82562ET /82562EM	C	
Dual Layout Footprint	D	

9.10.1. ICH3-M – LAN Connect Interface (LCI) Guidelines

This section contains guidelines on how to implement a PLC (Platform LAN Connect) device on a system motherboard using LAN Connect Interface (LCI). It should not be treated as a specification and the system designer must ensure through simulations or other techniques that the system meets the specified timings. Special care must be given to matching the LAN_CLK traces to those of the other signals, as shown below. The following are guidelines for the ICH3-M to LAN component interface. The following signal lines are used on this interface:

- LAN_CLK

- LAN_RSTSYNC
- LAN_RXD[2:0]
- LAN_TXD[2:0]

This interface supports both 82562EH and 82562ET/82562EM components. Signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD[0], and LAN_TXD[0] are shared by both components. Signal lines LAN_RXD[2:1] and LAN_TXD[2:1] are not connected when 82562EH is installed). Dual footprint guidelines are found in Figure 49 of this design guide.

9.10.1.1. Bus Topologies

The LAN Connect Interface can be configured in several topologies:

- Direct point-to-point connection between the ICH3-M and the LAN component
- Dual Footprint
- LOM/CNR Implementation

9.10.1.2. Point-to-point Interconnect

The following are guidelines for a single solution motherboard. Either 82562EH, 82562ET, or CNR is installed.

Figure 50. Single Solution Interconnect

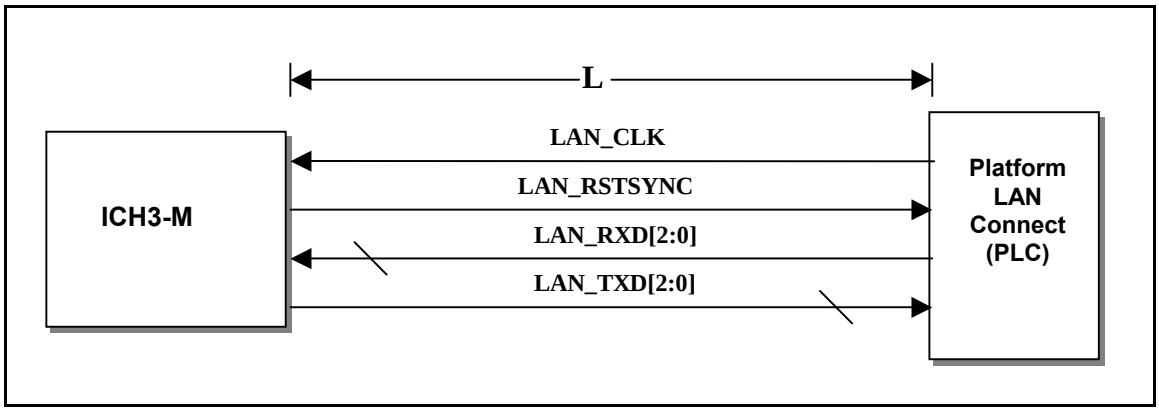


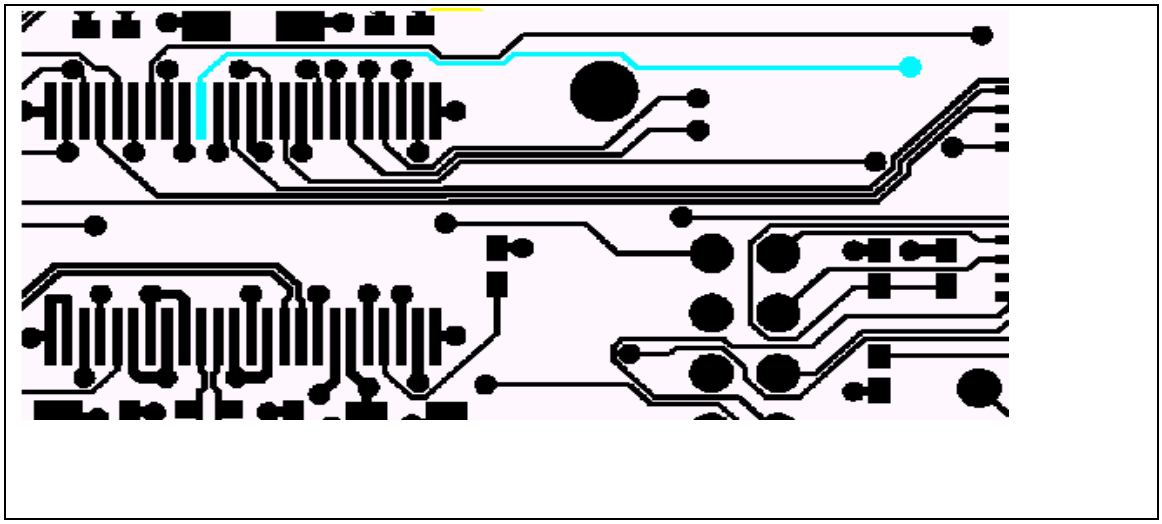
Table 38. LAN Design Guide Point-to-Point Length Requirements

Length Requirements From the Previous Figure	
Configuration:	A
82562EH	L = 4.5” to 10” (Signal Lines LAN_RXD[2:1] and LAN_TXD[2:1] not connected)
82562ET	L = 3.5” to 10”
CNR	L = 3” to 9” (0.5” to 3” on card)

9.10.1.3. Signal Routing and Layout

Route the LAN Connect Interface (LCI) signals carefully on the motherboard to meet the timing and signal quality requirements of this interface specification. Designers should adhere to the following general guidelines. The board designer should simulate the board routing to verify that the specifications are met for flight times and skews due to trace mismatch and crosstalk. On the motherboard, the length of each data trace should be either equal in length to the LAN_CLK trace or up to 0.5 inches shorter than the LAN_CLK trace. (LAN_CLK should always be the longest motherboard trace in each group).

Figure 51. LAN_CLK Routing Example



9.10.1.4. Crosstalk Consideration

Noise due to crosstalk must be carefully controlled to a minimum. Crosstalk is the key cause of timing skews and is the largest part of the t_{RMATCH} skew parameter. t_{RMATCH} is the sum of the trace length mismatch between LAN_CLK and the LAN data signals. To meet this requirement on the board, the length of each data trace is either equal to or up to 0.5 inches shorter than the LAN_CLK trace. Maintaining at least 100 mils of spacing should minimize noise due to crosstalk from non-LCI signals.

9.10.1.5. Impedances

The motherboard impedances should be controlled to minimize the impact of any mismatch between the motherboard and the daughter card. An impedance of 60 Ω ± 10% is strongly recommended; otherwise, signal integrity requirements may be violated.

9.10.1.6. Line Termination

Line termination mechanisms are not specified for the LAN Connect Interface. Slew rate controlled output buffers achieve acceptable signal integrity by controlling signal reflection, over/undershoot, and ringback. A 33-Ω series resistor can be installed at the driver side of the interface should the developer have concerns about over/undershoot. Note that the receiver must allow for any drive strength and board impedance characteristic within the specified ranges.

9.10.2. General LAN Routing Guidelines and Considerations

9.10.2.1. General Trace Routing Considerations

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes.

Observe the following suggestions to help optimize board performance (Note: Some suggestions are specific to a 4.5-mil stackup.):

- Maximum mismatch between the length of the clock trace and the length of any data trace is 0.5 inches (clock trace must be longest). See Table 39 for summary of Recommendations
- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths of a differential pair equal to each other.
- Keep the total length of each differential pair under 4 inches. [Many customer designs with differential traces longer than 5 inches have had one or more of the following issues: IEEE phy conformance failures, excessive EMI, and/or degraded receive BER.]
- Do not route the transmit differential traces closer than 100 mils to the receive differential traces.
- Do not route any other signal traces both parallel to the differential traces, and closer than 100 mils to the differential traces (300 mils is recommended).
- Keep maximum separation between differential pairs to 7 mils.
- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90° bend is required, it is recommended to use two 45° bends instead.
- Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.

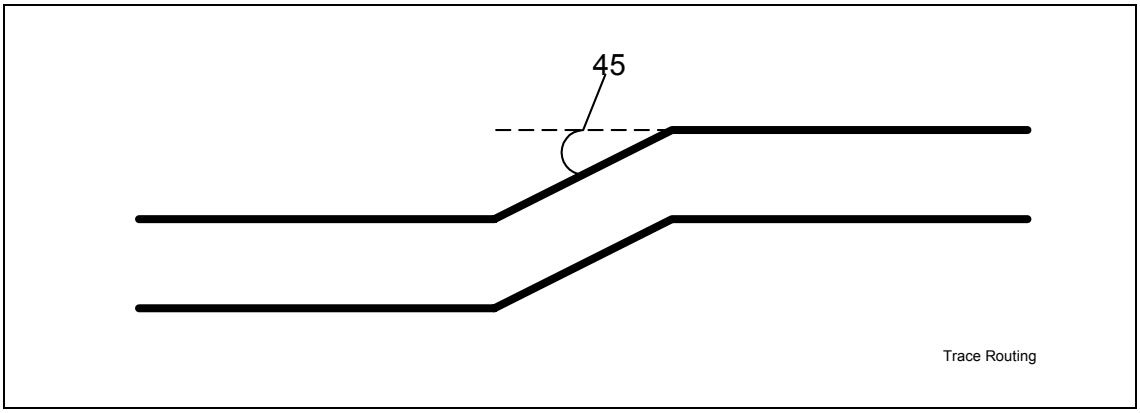
Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

Table 39. LAN Signals

Signal	Max length (inch)	Width (mils)	Space btwn diff pair (mils)	Space btwn trans. recv. diff pair or other signals(mils)	Mismatch relative max. (mils)	Relative To	Notes
Signals Group#lan1 LAN_RXD0 to LAN_RXD2 LAN_TXD0 to LAN_TXD2 LAN_RST	11 (min 3.5)	5	*5	8	-500	LAN_JCLK	Diff. Pair must be the same length (± 10 mils) Trace width is 5 mils Trace spacing is 7 mils
Signals Group#lan2 TDP (pin9, J23A) TDN (pin10, J23A) LAN_RDP LAN_RDN LAN_JCL	4	5	7	70	+/-10	Signals Group# an 2 diff pair	Diff. Pair must be the same Length (±10 mils) Trace width is 5 mils Trace spacing is 7 mils
LAN_JCLK	11 (min 3.5)	5	None	16	+500	Signals Group#lan1	LAN_JCLK is equal to Signals Group#lan1 or longer by 500 mil (max)

NOTE: * This parameter is not for diff pairs, it is the space between data lines.

Figure 52. Trace Routing



9.10.2.1.1. Trace Geometry and Length

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, this trace

width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane. Differential trace impedances should be controlled to be ~100 Ω. It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by up to 10 Ω, when the traces within a pair are closer than 30 mils (edge to edge).

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. Also for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance. Additionally, the PLC should not be closer than one inch to the connector/magnetics/edge of the board.

9.10.2.1.2. Signal Isolation

Some rules to follow for signal isolation:

- Separate and group signals by function on separate layers if possible. Maintain a gap of 100 mils between all differential pairs (Phoneline and Ethernet) and other nets, but group associated differential pairs together. Note: Over the length of the trace run, each differential pair should be at least 0.3 inches away from any parallel signal traces.
- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN or Phoneline traces near other high-frequency signals associated with a video controller, cache controller, CPU, or other similar devices.

9.10.2.2. Power and Ground Connections

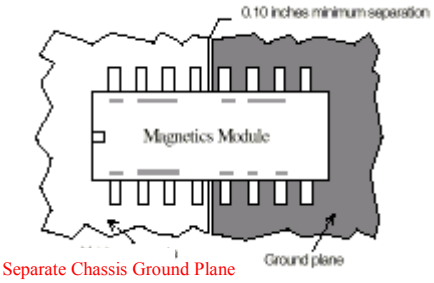
Some rules and guidelines to follow for power and ground connections:

- All Vcc pins should be connected to the same power supply.
- All Vss pins should be connected to the same ground plane.
- Four to six decoupling capacitors, including two 4.7-µF capacitors are recommended
- Place decoupling as close as possible to power pins.

9.10.2.2.1. General Power and Ground Plane Considerations

To properly implement the common mode choke functionality of the magnetics module the chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum.

Figure 53. Ground Plane Separation



Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return, will significantly reduce EMI radiation.

Some rules to follow that will help reduce circuit inductance in both backplanes and motherboards.

- Route traces over a continuous plane with no interruptions (do not route over a split plane). If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.
- Separate noisy digital grounds from analog grounds to reduce coupling.
- Noisy digital grounds may affect sensitive DC subsystems.
- All ground vias should be connected to every ground plane; and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This will minimize the loop area.
- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high frequency harmonics that can radiate EMI.
- The ground plane beneath the filter/transformer module should be split. The RJ45 and/or RJ11 connector side of the transformer module should have chassis ground beneath it. By splitting ground planes beneath transformer, noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer is minimized. There should not be a power plane under the magnetics module.
- Create a spark gap between pins 2 through 5 of the Phoneline connector(s) and shield ground of 1.6 mm (59.0 mil). This is a **critical** requirement needed to past FCC part 68 testing for phoneline connection.

  NOTE: For worldwide certification, a trench of 2.5 mm is required. In North America, the spacing requirement is 1.6 mm. However, home networking can be used in other parts of the world, including Europe, where some Nordic countries require the 2.5 mm spacing.

9.10.2.3. A Four-Layer Board Design (Example)

9.10.2.3.1. Top Layer Routing

Sensitive analog signals are routed completely on the top layer without the use of vias. This allows tight control of signal integrity and removes any impedance inconsistencies due to layer changes.

9.10.2.3.2. Ground Plane

A layout split (100 mils) of the ground plane under the magnetics module between the primary and secondary side of the module is recommended. It is also recommended to minimize the digital noise injected into the 82562 common ground plane. Suggestions include optimizing decoupling on neighboring noisy digital components, isolating the 82562 digital ground using a ground cutout, etc.

9.10.2.3.3. Power Plane

Physically separate digital and analog power planes must be provided to prevent digital switching noise from being coupled into the analog power supply planes VDD_A. Analog power may be a metal fill "island", separated from digital power, RC filtered from the digital power.

9.10.2.3.4. Bottom Layer Routing

The digital high-speed signals that include all of the LAN interconnect interface signals are routed on the bottom layer.

9.10.2.4. Common Physical Layout Issues

Here is a list of common physical layer design and layout mistakes in LAN On Motherboard Designs.

- Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and will distort the transmit or receive waveforms.
- Lack of symmetry between the two traces within a differential pair. [Each component and/or via that one trace encounters, the other trace must encounter the same component or a via at the same distance from the PLC.] Asymmetry can create common-mode noise and distort the waveforms.
- Excessive distance between the PLC and the magnetics or between the magnetics and the RJ-45/11 connector. Beyond a total distance of about 4 inches, it can become extremely difficult to design a spec-compliant LAN product. Long traces on FR4 (fiberglass epoxy substrate) will attenuate the analog signals. Also, any impedance mismatch in the traces will be aggravated if they are longer (see bullet #9 below). The magnetics should be as close to the connector as possible (less than or equal to one inch).
- Routing any other trace parallel to and close to one of the differential traces. Crosstalk getting onto the receive channel will cause degraded long cable BER. Crosstalk getting onto the transmit channel can cause excessive emissions (failing FCC) and can cause poor transmit BER on long cables. At a minimum, other signals should be kept 0.3 inches from the differential traces.
- Routing the transmit differential traces next to the receive differential traces. The transmit trace that is closest to one of the receive traces will put more crosstalk onto the closest receive trace and can greatly degrade the receiver's BER over long cables. After exiting the PLC, the transmit traces should be kept 0.3 inches or more away from the nearest receive trace. The only possible exceptions are in the vicinities where the traces enter or exit the magnetics, the RJ-45/11, and the PLC.
- Use of an inferior magnetics module. The magnetics modules that we use have been fully tested for IEEE PLC conformance, long cable BER, and for emissions and immunity. (Inferior magnetics modules often have less common-mode rejection and/or no auto transformer in the transmit channel.)

- Use of an 82555 or 82558 physical layer schematic in a PLC design. The transmit terminations and decoupling are different. There are also differences in the receive circuit. For appropriate reference schematic or Application-Note, please consult Intel Field Application Engineers.
- Not using (or incorrectly using) the termination circuits for the unused pins at the RJ-45/11 and for the wire-side center-taps of the magnetics modules. These unused RJ pins and wire-side center-taps must be correctly referenced to chassis ground via the proper value resistor and a capacitance or termplane. If these are not terminated properly, there can be emissions (FCC) problems, IEEE conformance issues, and long cable noise (BER) problems. The Application Notes have schematics that illustrate the proper termination for these unused RJ pins and the magnetics center-taps. Please consult Intel FAE for the availability of the reference materials.
- Incorrect differential trace impedances. It is important to have ~100 Ω impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. It is very common to see customer designs that have differential trace impedances between 75 Ω and 85 Ω, even when the designers think they've designed for 100 Ω. [To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close† to each other the edge coupling can lower the effective differential impedance by 5 to 20 Ω. A 10-Ω to 15-Ω drop in impedance is common] Short traces will have fewer problems if the differential impedance is a little off.
- Use of capacitor that is too large between the transmit traces and/or too much capacitance from the magnetic's transmit center-tap (on the 82562ET side of the magnetics) to ground. Using capacitors more than a few pF in either of these locations can slow the 100 Mbps rise and fall time so much that they fail the IEEE rise time and fall time specs. This will also cause return loss to fail at higher frequencies and will degrade the transmit BER performance. Caution should be exercised if a cap is put in either of these locations. If a cap is used, it should almost certainly be less than 22 pF. [6 pF to 12 pF values have been used on past designs with reasonably good success.] These caps are not necessary, unless there is some overshoot in 100 Mbps mode.

Note: It is important to keep the two traces within a differential pair close† to each other. Keeping them close† helps to make them more immune to crosstalk and other sources of common-mode noise. This also means lower emissions (i.e. FCC compliance) from the transmit traces, and better receive BER for the receive traces.

Note: † Close should be considered to be less than 0.030 inches between the two traces within a differential pair. 0.007 inch trace-to-trace spacing is recommended.

9.10.3. 82562EH Home/PNA* Guidelines

For correct LAN performance, designers must follow the general guidelines outlined in Section 9.10.2. General LAN Routing Guidelines and Considerations. Additional guidelines for implementing an 82562EH Home/PNA* Platform LAN Connect component are provided below.

9.10.3.1. Power and Ground Connections

Some rules to follow for power and ground connections:

- For best performance place decoupling capacitors on the backside of the PCB directly under the 82562EH with equal distance from both pins of the capacitor to power/ground.

- The analog power supply pins for 82562EH (VCCA, VSSA) should be isolated from the digital VCC and VSS through the use of ferrite beads. In addition, adequate filtering and decoupling capacitors should be provided between VCC and VSS, and VCCA, and VSSA power supplies.

9.10.3.2. Guidelines for 82562EH Component Placement

Component placement can affect signal quality, emissions, and temperature of a board design. This section will provide guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet FCC specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the HomePNA* LAN interface is important because all other interface will compete for physical space on a motherboard near the connector edge. As with most subsystems, the HomePNA* LAN circuits need to be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

9.10.3.3. Crystals and Oscillators

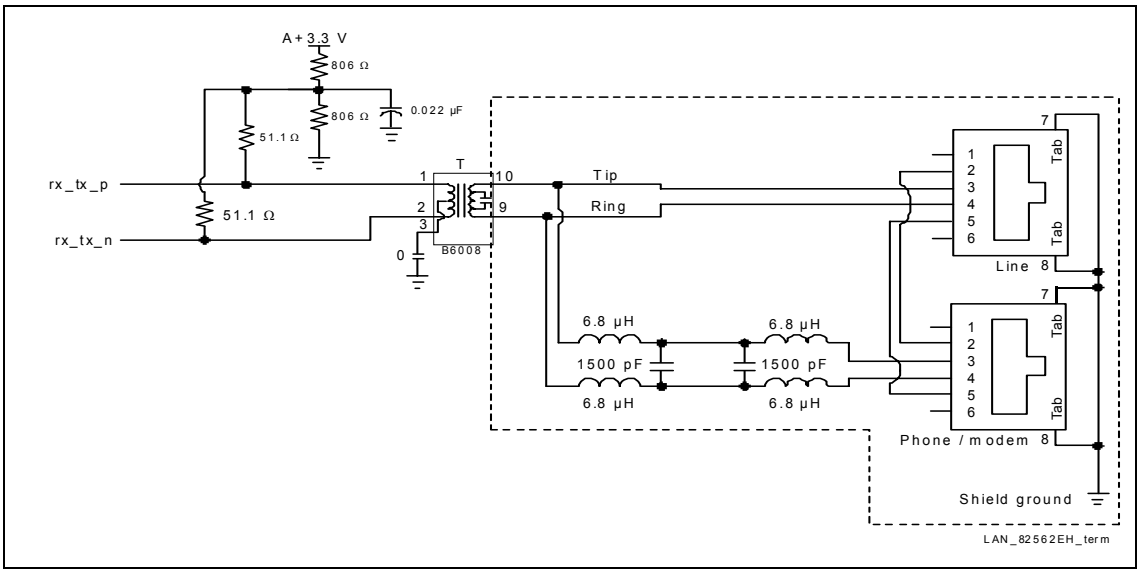
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the HomePNA* magnetics module to prevent interference of communication. The retaining straps of the crystal (if they should exist) should be grounded to prevent possibility radiation from the crystal case and the crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For a noise free and stable operation, place the crystal and associated discretes as close as possible to 82562EH, keeping the length as short as possible and do not route any noisy signals in this area.

9.10.3.4. Phoneline HPNA Termination

The transmit/receive differential signal pair is terminated with a pair of 51.1Ω (1%) resistors. This parallel termination should be placed close to the 82562EH. The center, common point between the 51.1-ohm resistors is connected to a voltage divider network. The opposite end of one 806Ω resistor is tied to VCCA (3.3V), and the opposite end of the other 806-Ω resistor and the cap are connected to ground. The termination is shown in the following figure.

Figure 54. 82562EH Termination



The filter and magnetics component T1, integrates the required filter network, high-voltage impulse protection, and transformer to support the HomePNA* LAN interface.

One RJ-11 jack (labeled “LINE” in the above figure) allows the node to be connected to the phoneline, and the second jack (labeled “PHONE” in the above figure) allows other downline devices to be connected at the same time. This second connector is not required by HomePNA*. However, typical PCI adapters and PC motherboard implementations are likely to include it for user convenience.

A low-pass filter, setup in-line with the second RJ-11 jack is also recommended by the HomePNA* to minimize interference between the HomeRun connection and a POTs voice or modem connection on the second jack. This places a restriction of the type of devices connected to the second jack as the pass-band of this filter is set approximately at 1.1 MHz. Please refer to the HomePNA* website: www.homepna.org for up-to-date information and recommendations regarding the use of this low-pass filter to meet HomePNA* certifications.

9.10.3.5. Critical Dimensions

There are three dimensions to consider during layout. Distance ‘A’ from 82562EH to the magnetics module, distance ‘B’ from the line RJ11 connector to the magnetics module, and distance ‘C’ from the phone RJ11 to the LPF (if implemented).

Figure 55. Critical Dimensions for Component Placement

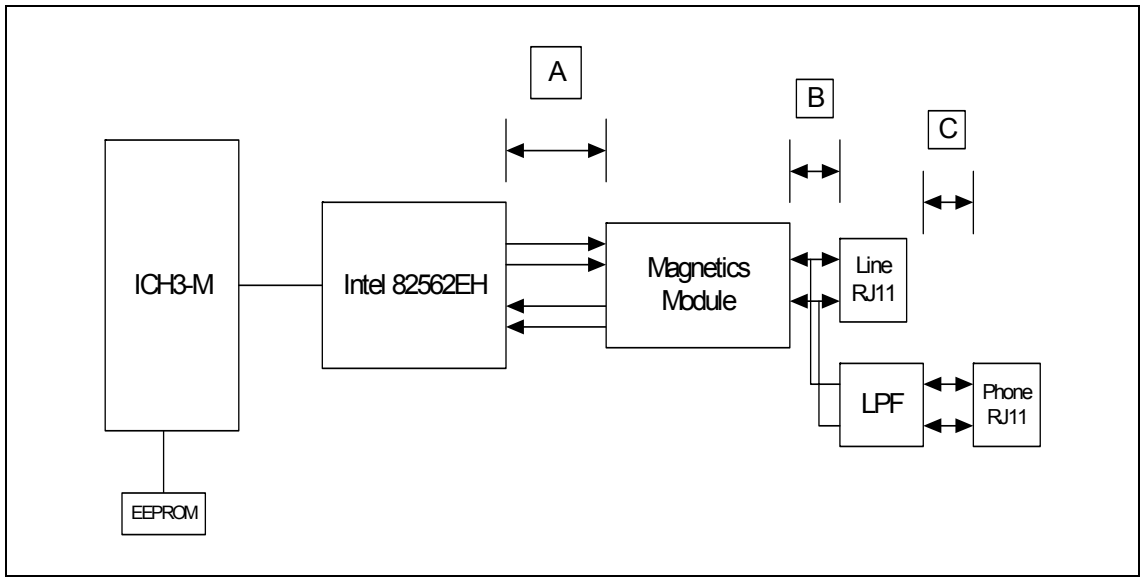


Table 40. 82562EH Home/PNA* Critical Dimensions for Component Placement

Distance	Priority	Guideline
B	1	< 1 inch
A	2	< 1 inch
C	3	< 1 inch

9.10.3.5.1. Distance from Magnetics Module to Line RJ11

This distance ‘B’ should be given highest priority and should be less then 1 inch. In regards to trace symmetry, route differential pairs with consistent separation and with exactly the same lengths and physical dimensions.

Asymmetrical and unequal length in the differential pairs contribute to common mode noise and this can degrade the receive circuit performance and contribute to radiated emissions from the transmit side.

9.10.3.5.2. Distance from 82562EH to Magnetics Module

Due to the high-speed of signals present, distance ‘A’ between the 82562EH and the magnetics should also be less than 1 inch, but should be second priority relative to distance form connects to the magnetics module.

And in general, any section of trace that is intended for use with high-speed signals should observe proper termination practices. Proper signal termination can reduce reflections caused by impedance mismatches between device and traces route. The reflections of a signal may have a high-frequency component that may contribute more EMI than the original signal itself.

9.10.3.5.3. Distance from LPF to Phone RJ11

This distance 'C' should be less then 1 inch. In regards to trace symmetry, route differential pairs with consistent separation and with exactly the same lengths and physical dimensions.

Asymmetrical and unequal length in the differential pairs contribute to common mode noise and this can degrade the receive circuit performance and contribute to radiated emissions from the transmit side.

9.10.4. 82562ET / 82562EM Guidelines

For correct LAN performance, designers must follow the general guidelines outlined in Section 9.10.2. General LAN Routing Guidelines and Considerations. Additional guidelines for implementing an 82562ET or 82562EM Platform LAN Connect component are provided below.

9.10.4.1. Guidelines for 82562ET / 82562EM Component Placement

Component placement can affect signal quality, emissions, and temperature of a board design. This section will provide guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet FCC and IEEE test specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the Ethernet LAN interface is important because all other interface will compete for physical space on a motherboard near the connector edge. As with most subsystems, the Ethernet LAN circuits need to be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

9.10.4.2. Crystals and Oscillators

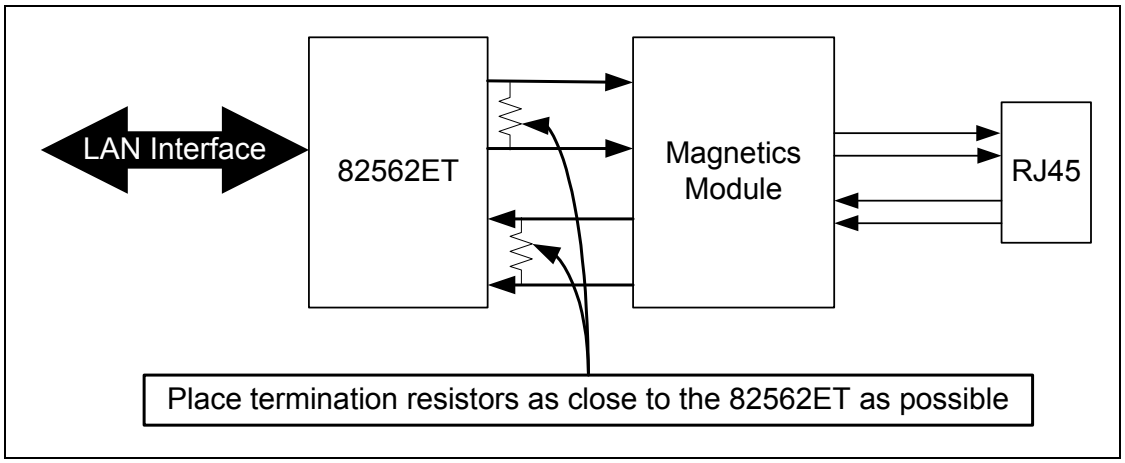
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the Ethernet magnetics module to prevent interference of communication. The retaining straps of the crystal (if they should exist) should be grounded to prevent possibility radiation from the crystal case and the crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For a noise free and stable operation, place the crystal and associated discretes as close as possible to the 82562ET or 82562EM, keeping the trace length as short as possible and do not route any noisy signals in this area.

9.10.4.3. 82562ET / 82562EM Termination Resistors

The 100-Ω (1%) resistor used to terminate the differential transmit pairs (TDP/TDN) and the 100-Ω (1%) receive differential pairs (RDP/RDN) should be placed as close to the Platform LAN Connect component (82562ET or 82562EM) as possible. This is due to the fact these resistors are terminating the entire impedance that is seen at the termination source (i.e. 82562ET), including the wire impedance reflected through the transformer.

Figure 56. 82562ET/82562EM Termination



9.10.4.4. Critical Dimensions

There are two dimensions to consider during layout. Distance 'B' from the line RJ45 connector to the magnetics module and distance 'A' from the 82562ET or 82562EM to the magnetics module. The combined total distances A and B must not exceed 4 inches (preferably, less than 2 inches.) See the following figure.

Figure 57. Critical Dimensions for Component Placement

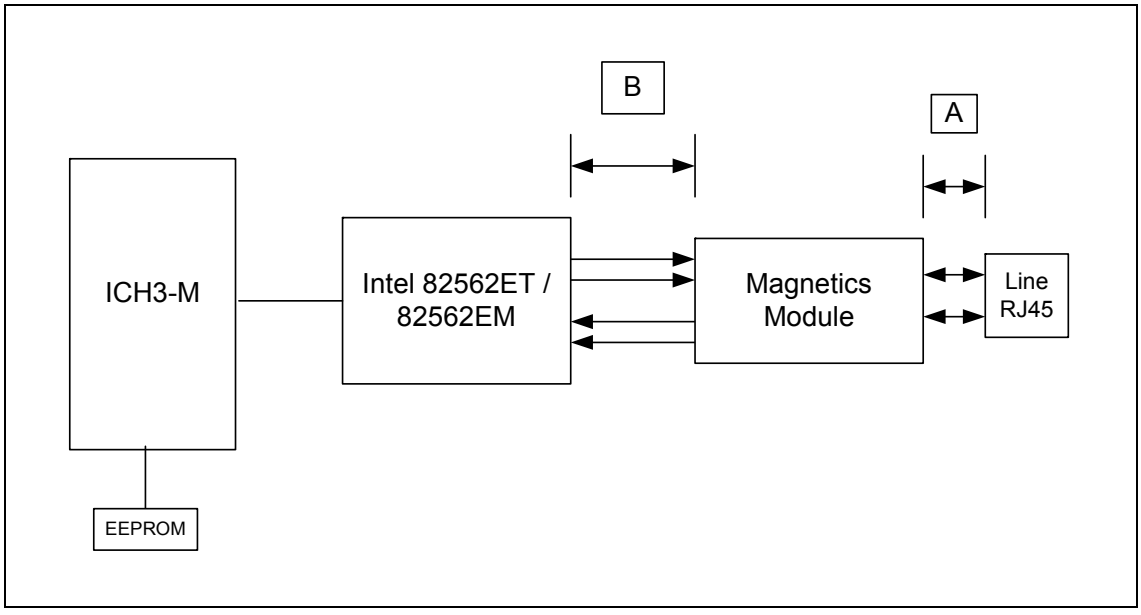


Table 41. 82562ET / 82562EM Critical Dimensions for Component Placement

Distance	Priority	Guideline
A	1	< 1 inch
B	2	< 1 inch

9.10.4.4.1. Distance from Magnetics Module to RJ45

The distance A in the above figure should be given the highest priority in board layout. The distance between the magnetics module and the RJ45 connector should be kept to less than one inch of separation. The following trace characteristics are important and should be observed:

- Differential Impedance: The differential impedance should be 100 Ω. The single ended trace impedance will be approximately 50 Ω; however, the differential impedance can also be affected by the spacing between the traces.
- Trace Symmetry: Differential pairs (such as TDP and TDN) should be routed with consistent separation and with exactly the same lengths and physical dimensions (for example, width).

Caution: Asymmetric and unequal length traces in the differential pairs contribute to common mode noise. This can degrade the receive circuit's performance and contribute to radiated emissions from the transmit circuit. If the 82562ET must be placed further than a couple of inches from the RJ45 connector, distance B can be sacrificed. Keeping the total distance between the 82562ET and RJ-45 will as short as possible should be a priority.

Note: Measured trace impedance for layout designs targeting 100 Ω often result in lower actual impedance. OEMs should verify actual trace impedance and adjust their layout accordingly. If the actual impedance is consistently low, a target of 105 Ω -110 Ω should compensate for second order effects.

9.10.4.4.2. Distance from 82562ET to Magnetics Module

Distance B should also be designed to be less than one inch between devices. The high-speed nature of the signals propagating through these traces requires that the distance between these components be closely observed. In general, any section of traces that is intended for use with high-speed signals should observe proper termination practices. Proper termination of signals can reduce reflections caused by impedance mismatches between device and traces. The reflections of a signal may have a high frequency component that may contribute more EMI than the original signal itself. For this reason, these traces should be designed to a 100-Ω differential value. These traces should also be symmetric and equal length within each differential pair.

9.10.4.5. Reducing Circuit Inductance

The following guidelines show how to reduce circuit inductance in both back planes and motherboards. Traces should be routed over a continuous ground plane with no interruptions. If there are vacant areas on a ground or power plane, the signal conductors should not cross the vacant area. This increases inductance and associated radiated noise levels. Noisy logic grounds should be separated from analog signal grounds to reduce coupling. Noisy logic grounds can sometimes affect sensitive DC subsystems such as analog to digital conversion, operational amplifiers, etc. All ground vias should be connected to every ground plane; and similarly, every power via, to all power planes at equal potential. This helps reduce circuit inductance. Another recommendation is to physically locate grounds to minimize the loop area between a signal path and its return path. Rise and fall times should be as slow as possible because signals with fast rise and fall times contain many high frequency harmonics that can radiate significantly. The most sensitive signal returns closest to the chassis ground should be connected together. This will result in a smaller loop area and reduce the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk can be studied using electronics modeling software.

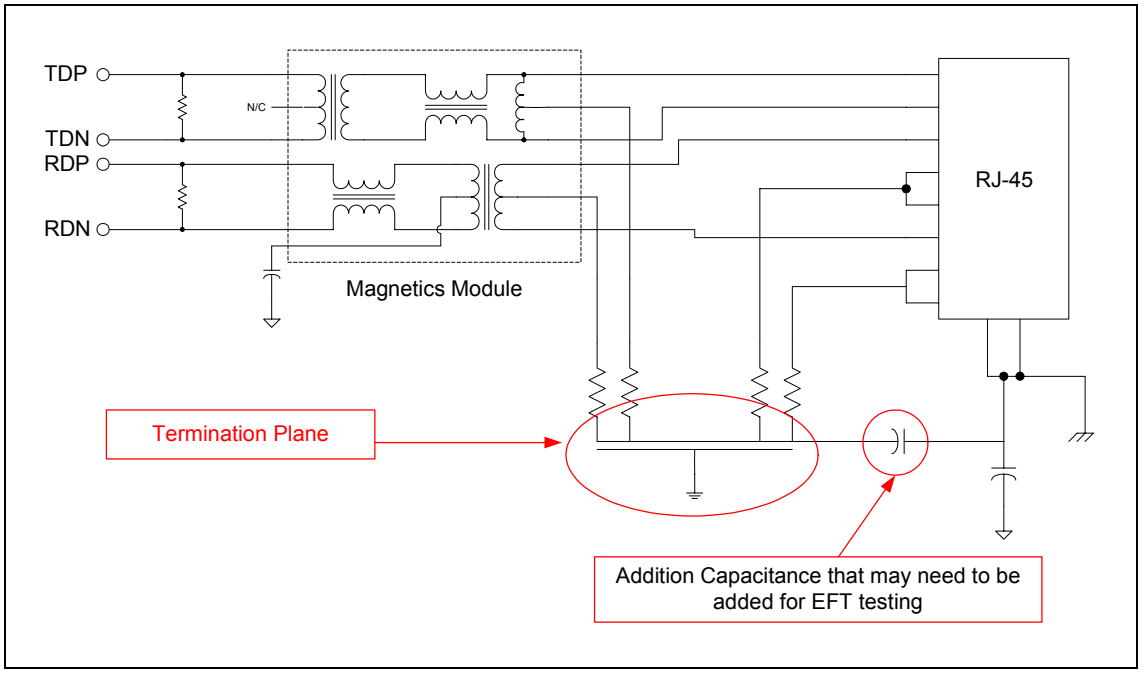
9.10.4.5.1. Terminating Unused Connections

In Ethernet designs it is common practice to terminate unused connections on the RJ-45 connector and the magnetics module to ground. Depending on overall shielding and grounding design, this may be done to the chassis ground, signal ground, or a termination plane. Care must be taken when using various grounding methods to insure that emission requirements are met. The method most often implemented is called the “Bob Smith” Termination. In this method a floating termination plane is cut out of a power plane layer. This floating plane acts as a plate of a capacitor with an adjacent ground plane and couples to the ground plane creating the required 1500 pF of capacitance. The signals can be routed through 75-Ω resistors to the plane. Stray energy on unused balls is then carried to the plane.

9.10.4.5.2. Termination Plane Capacitance

Intel recommends that the termination plane capacitance equal a minimum value of 1500 pF. This helps reduce the amount of crosstalk on the differential pairs (TDP/TDN and RDP/RDN) from the unused pairs of the RJ45. Pads may be placed for an additional capacitance to chassis ground, which may be required if the termplane capacitance is not large enough to pass EFT (Electrical Fast Transient) testing. If a discrete capacitor is used, to meet the EFT requirements it should be rated for at least 1000 Vac.

Figure 58. Termination Plane



9.10.5. 82562ET / 82562EH Dual Footprint Guidelines

These guidelines characterize the proper layout for a dual footprint solution. This configuration enables the developer to install either the 82562EH or the 82562ET/82562EM components while having only one motherboard design. The following are guidelines for the 82562ET/82562EH Dual Footprint option. The dual footprint for this particular solution uses a SSOP footprint for 82562ET and a TQFP footprint for 82562EH. The combined footprint for this configuration is shown in the below two figures.

Figure 59. Dual Footprint LAN Connect Interface

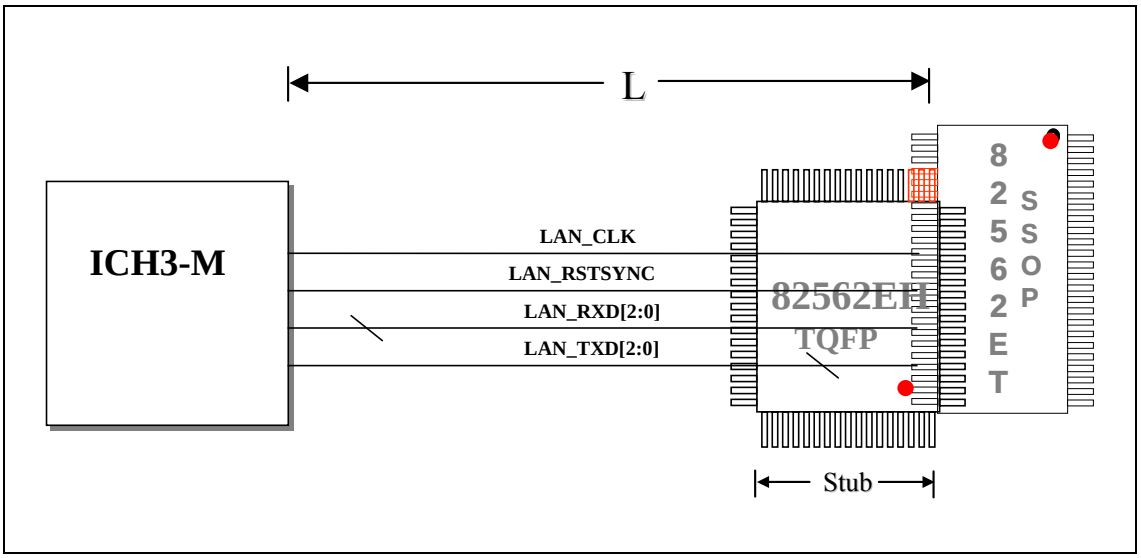
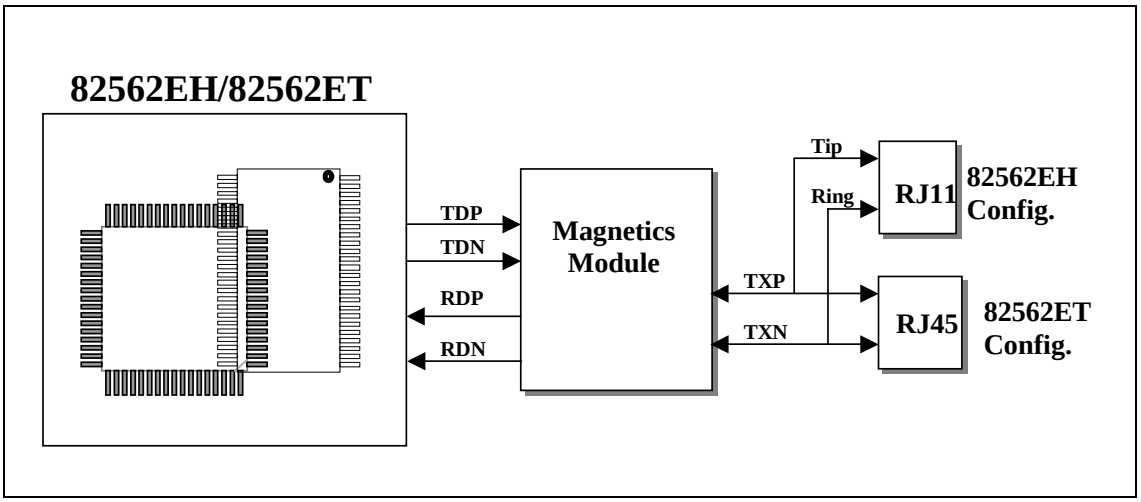


Figure 60. Dual Footprint Analog Interface



The following are additional guidelines for this configuration:

- L = 0.5 inches to 6.5 inches
- Stub < 0.5 inches
- Either 82562EH or 82562ET/82562EM can be installed. Not both
- 82562ET pins 28,29, and 30 overlap with 82562EH pins 17,18, and 19.
- Overlapping pins are tied to ground.
- No other signal pads should overlap or touch.
- The 82562EH and 82562ET configurations share signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD[0], LAN_TXD[0], RDP, RDN, RXP/Ring, and RXN/Tip.
- No stubs should be present when 82562ET is installed.
- Packages used for the Dual Footprint are TQFP for 82562EH and SSOP for 82562ET.

- A 22-Ω resistor can be placed at the driving side of the signal line to improve signal quality on the LAN connect interface.
- Resistor should be placed as close as possible to the component.
- Use components that can satisfy both the 82562ET and 82562EH configurations (i.e. magnetics module).
- Install components for either the 82562ET or the 82562EH configuration. Only one configuration can be installed at a time.
- Route shared signal lines such that stubs are not present or are kept to a minimum.
- Stubs may occur on shared signal lines (i.e. RDP and RDN). These stubs are due to traces routed to an uninstalled component. In an optimal layout, there should be no stubs.
- Use 0-Ω resistors to connect and disconnect circuitry not shared by both configurations. Place resistor pads along the signal line to reduce stub lengths.
- Traces from magnetics to connector must be shared and not stubbed. An RJ-11 connector that fits into the RJ-45 slot is available. Any amount of stubbing will destroy both HomePNA* and Ethernet performance.

10. Clocking

10.1. Clock Routing Guidelines

Table 42. Trace Length Overview

Clock Group	Topology Fig#	Length of Trace A	Length of Trace B	Length of Trace C	Refdes for Resistors in Topology and Their Values in Ω
HOST_CLK*	1	2.5 to 10	0 to 0.25	NA	R1 = 63.2, R2 = 33, R3 =470**
GBOUT_66	3	0 to 0.5	2 to 8.5	NA	R1 = 50
CLK66	4	0 to 0.5	X	NA	R1 = 33
AGPCLK	5	0 to 0.5	X		R1 = 33 (Note 1)
AGPCLK	5	0 to 0.5	X-4	4	R1 = 33 (Note 2)
CLK33	6	0 to 0.5	X	NA	R1 = 33 (Note 1)
PCICLK	7	0 to 0.5	X	NA	R1 = 33 (Note 1)
DOT_CLOCK	8	0 to 0.5	1.5 to 7.5	NA	R1 = 22
USB_CLOCK	TBD	TBD	TBD	TBD	TBD
APIC_CLK @ CPU	9	0 to 0.25	4 to 11.5	TBD	R1=33, R2=27, R3=138.
APIC_CLK @ ICH3-M	10	0 to 0.25	4 to 11.5	TBD	R1=33, R2=50, R3=350

NOTES:
1. * Routing for this clock group needs special attention. Please check the appropriate section for details.
2. ** Use 1% tolerance resistors for R1, R2, R3, Rs1, and Rs2.

The trace impedance in each case except in the clock group HOST_CLK is assumed to be 55 Ohms ± 15%. As for the trace impedance in case of HOST_CLK, use differential impedance of 100 Ohms ± 10 %, and a single-ended odd-mode impedance of 50 Ohms.

Note: 1:The recommended range for X, as defined in table 29 is from 2 to 8.5 inches. The value X should be length matched to Trace B (Figure 63) of the CLK66 group. Intel recommends to simulate the maximum trace mismatch based on the board stackup and routing requirement.

Note: 2: If an AGP connector is used total trace length from the Intel 830MP/830M Chipset GMCH-M to Graphics controller must meet Trace B requirements. Recommendation is GMCH-M to connector be X-4 inches and from connector to graphic device to be 4 inches and must meet the CLK66 Trace B trace length requirement.

The clocks are being classified into various groups per their frequency and topology and are show in Table 43.

Table 43. Clock Groups

Clock Name	Frequency	Receivers	Drivers
HOST_CLK	133 MHz	CPU, GMCH-M	CK-408
GBOUT_66	66 MHz	CK-408	GMCH-M
CLK66	66 MHz	GMCH-M, and ICH3-M	CK-408
AGPCLK	66 MHz	AGP Device (on AGP Card)	CK-408
CLK33	33 MHz	ICH3-M, FWH, SIO	CK-408
PCICLK	33 MHz	PCI Receivers (on PCI Cards)	CK-408
DOT_CLOCK	48 MHz	GMCH-M	CK-408
USB_CLOCK	48 MHz	ICH3-M	CK-408
APIC_CLK	33 MHz	CPU, ICH3-M	CK-408

10.1.1. HOST_CLK Clock Group

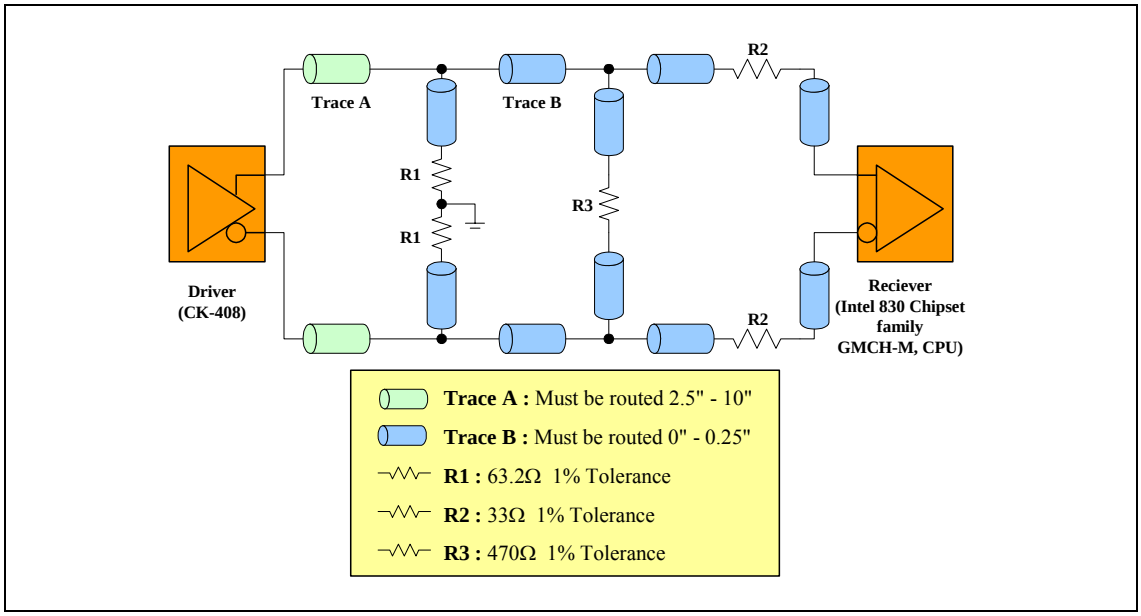
Given that both the input and output buffers are differential buffers, the traces are all considered to be buried microstrip_4 traces; with inner traces carrying the differential signals and the outer two traces connected to ground to give a good shield and to reduce EMI noise.

Trace impedance is 55 Ω ± 15% with 5 mil wide traces. Spacing to any other signals is 15 mils.

Differential impedance target 100 Ω with a spacing of 9 mils between the two signals.

Note: See Table 2 for pin-to-pin skew requirements. CPU and GMCH-M HOST_CLK trace length must meet these requirements. Intel recommends simulating the maximum trace mismatch based on the board stackup and routing requirement.

Figure 61. Topology for HOST_CLK

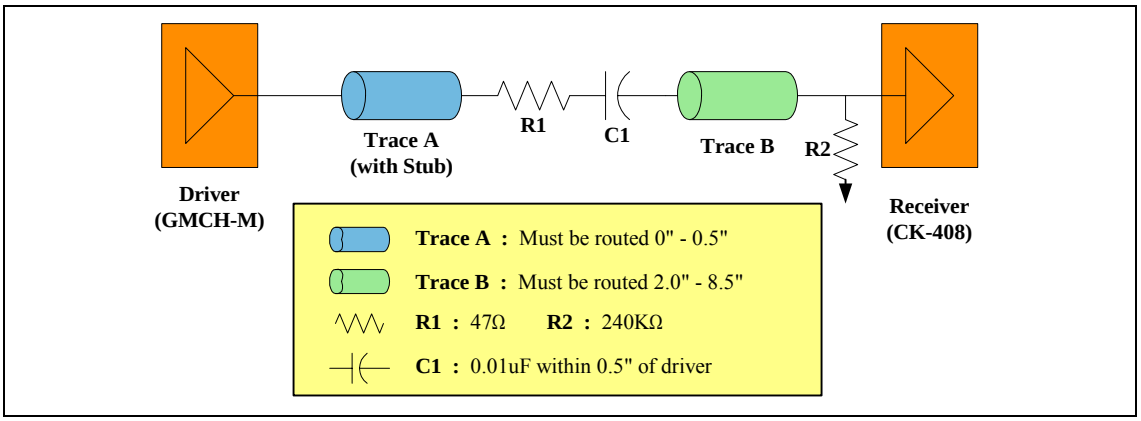


10.1.2. GBOUT_66 Clock Group

The driver is the Intel 830 Chipset family GMCH-M (GBOUT) 66-MHz clock output buffer and the receiver is 66-MHz clock input buffer at CK-408. *Note that this clock is asynchronous to all the other 66-MHz clocks on the system.*

Trace impedance is 55 Ω ± 15% with 5-mil wide traces. Spacing to any other signals is 15 mils.

Figure 62. Topology for GBOUT_66



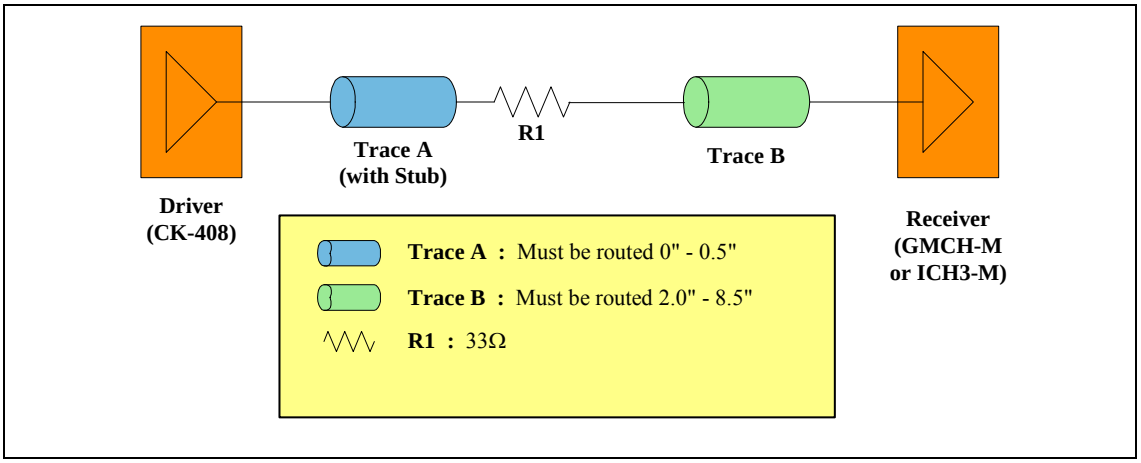
10.1.3. CLK66 Clock Group

The driver is the CK-408 66-MHz clock output buffer and the receiver is the 66-MHz clock input buffer at Intel 830 Chipset family GMCH-M (GBIN), and ICH3-M.

Note: Please refer to the latest revision of GMCH-M and ICH3-M Datasheet for required skew information if any.

Trace impedance is 55 Ω ± 15% with 5-mil wide traces. Spacing to any other signals is 15 mils.

Figure 63. Topology for CLK66



10.1.4. AGPCLK Clock Group (M/MP only)

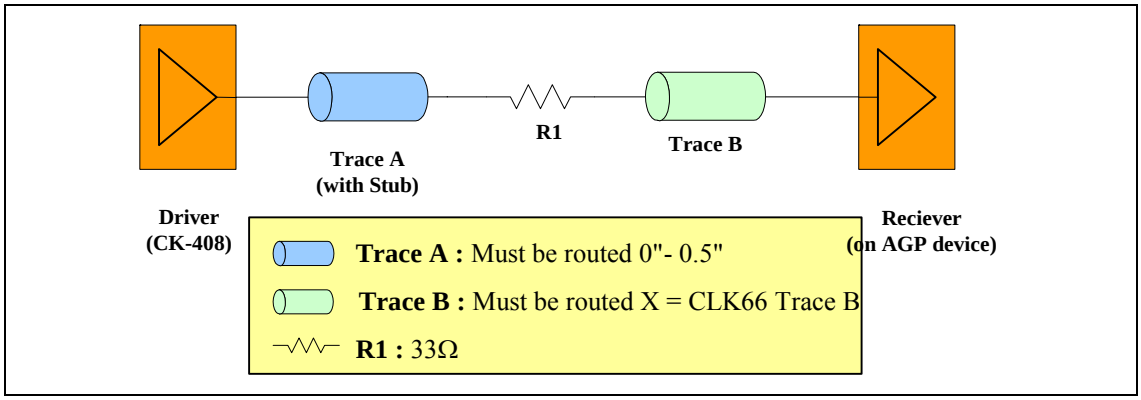
The driver is the CK-408 66-MHz clock output buffer and the receiver is the 66-MHz clock input buffer at the AGP device on the AGP device.

Note: Note: Please refer to the latest revision of GMCH-M and ICH3-M Datasheet for required skew information

Intel recommends stimulating this based on the board stackup and routing requirement.

Trace impedance is 55 Ω ± 15% with 5-mil wide traces. Spacing to any other signals is 15 mils.

Figure 64. Topology for AGPCLK



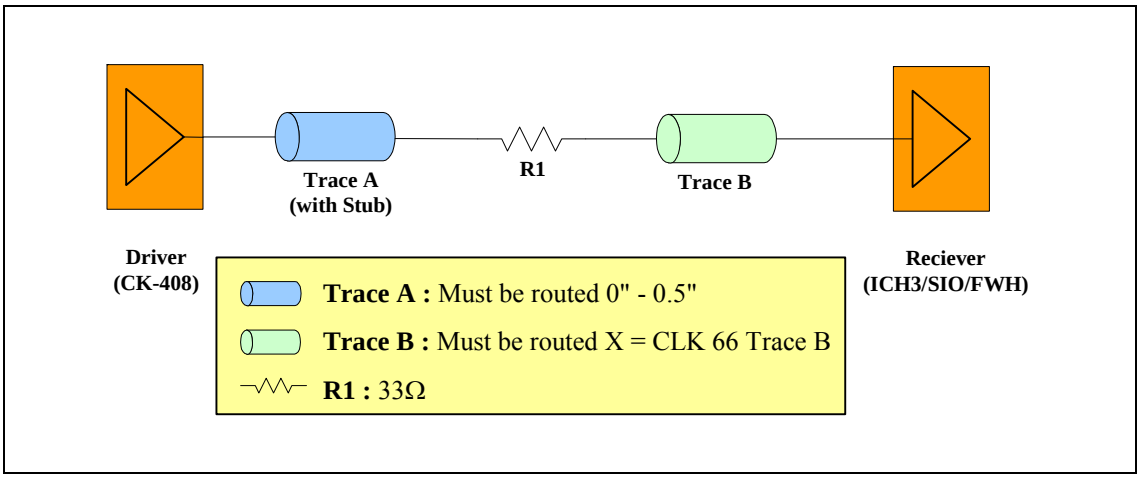
10.1.5. CLK33 Clock Group

The driver is the CK-408 33-MHz clock output buffer and the receiver is the 33-MHz clock input buffer at ICH3-M, FWH, and SIO.

Note: Please refer to the latest revision of ICH3-M Datasheet for required skew information if any. Intel recommends stimulating the maximum trace mismatch based on the board stackup and routing requirement.

The trace impedance is 55 Ω ± 15% with 5-mil wide traces. Spacing to any other signal is 15 mils.

Figure 65. Topology for CLK33



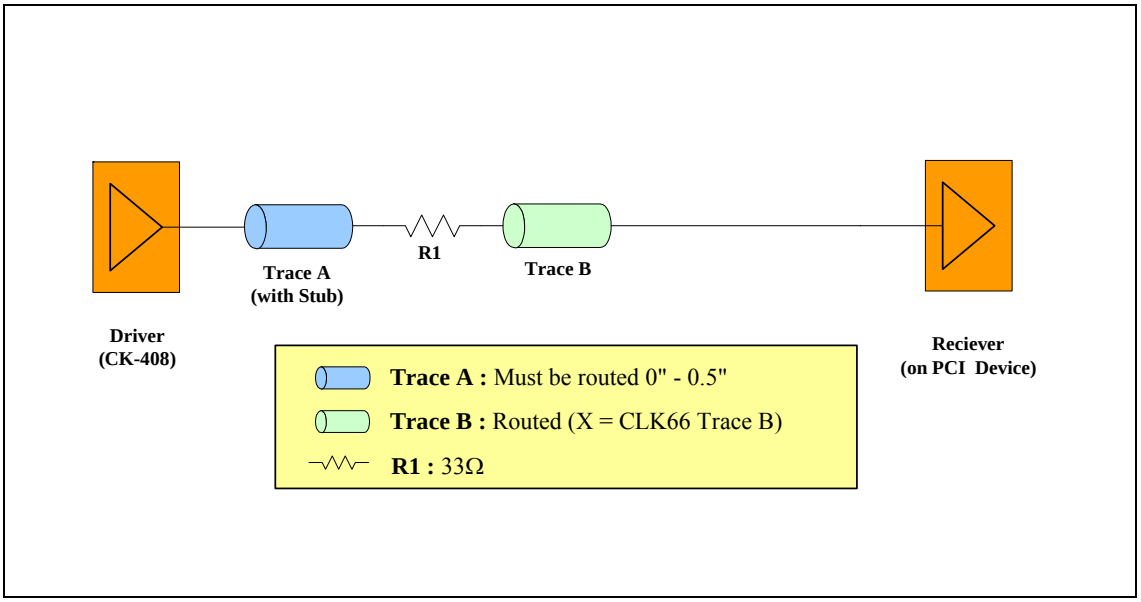
10.1.6. PCICLK Clock Group

The driver is the CK-408 33-MHz clock output buffer and the receiver is the 33-MHz clock input buffer at the PCI devices on the PCI cards.

Note: Please refer to the latest revision of ICH3-M Datasheet for required skew information.

Trace impedance is 55 Ω ± 15% with 5-mil wide traces. Spacing to any other signals is 15 mils.

Figure 66. Topology for PCICLK



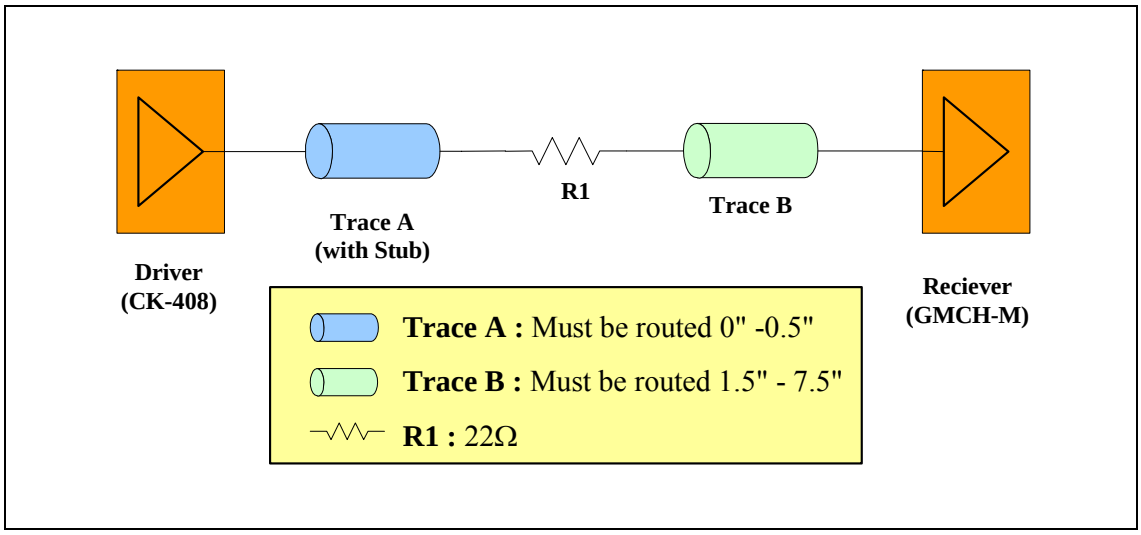
10.1.7. DOT_CLOCK Clock Group

The driver is the CK-408 dot clock output buffer and the receiver is the dot clock input buffer at the Intel 830 Chipset family GMCH-M.

Note: This clock is asynchronous to any other clock on the board.

Trace impedance is 55 Ω ± 15% with 5-mil wide traces. Spacing to any other signals is 15 mils.

Figure 67. Topology for DOT_CLOCK



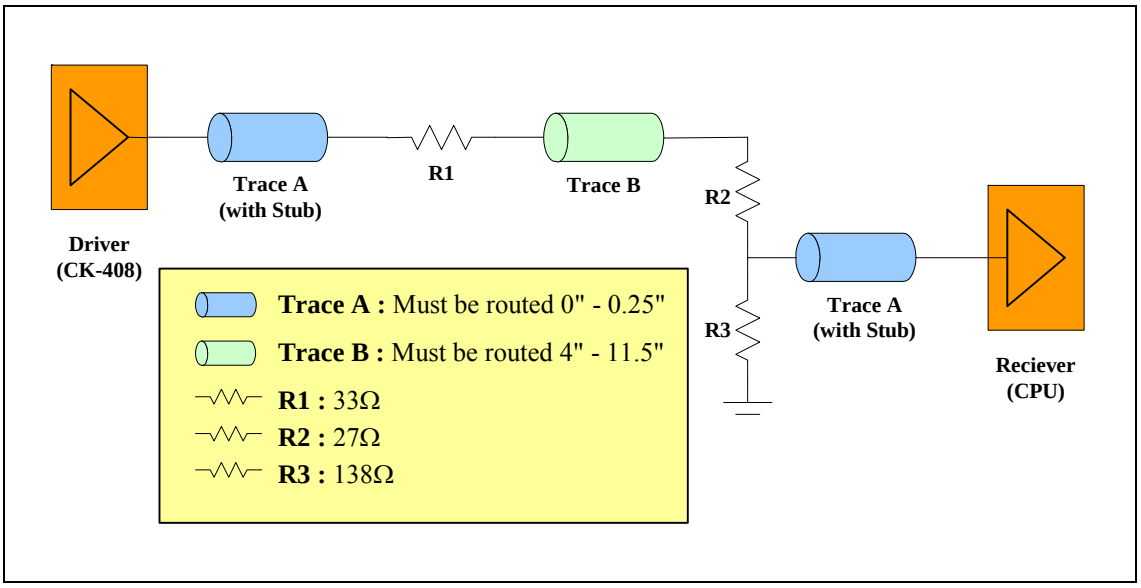
10.1.8. APIC_CLK Clock Group

The APIC_CLK signals are 33-MHz clocks driven by CK-408 and are received by the CPU and ICH3-M. The output available at the CK-408 pin is a LVTTL signal. Thus, given the voltage level requirement at each of the receivers is not LVTTL, a level shifter needs to be used. Also note that the voltage level requirement at each of the receivers is different from each other. Thus, each of these clocks will be discussed separately. These clocks do need to maintain a minimum skew between each other. However they, as a group, do not need to have any skew requirement with any other clocks in any other group.

Trace impedance is 55 Ω ± 15% with 5-mil wide traces. Spacing to any other signals is 15 mils.

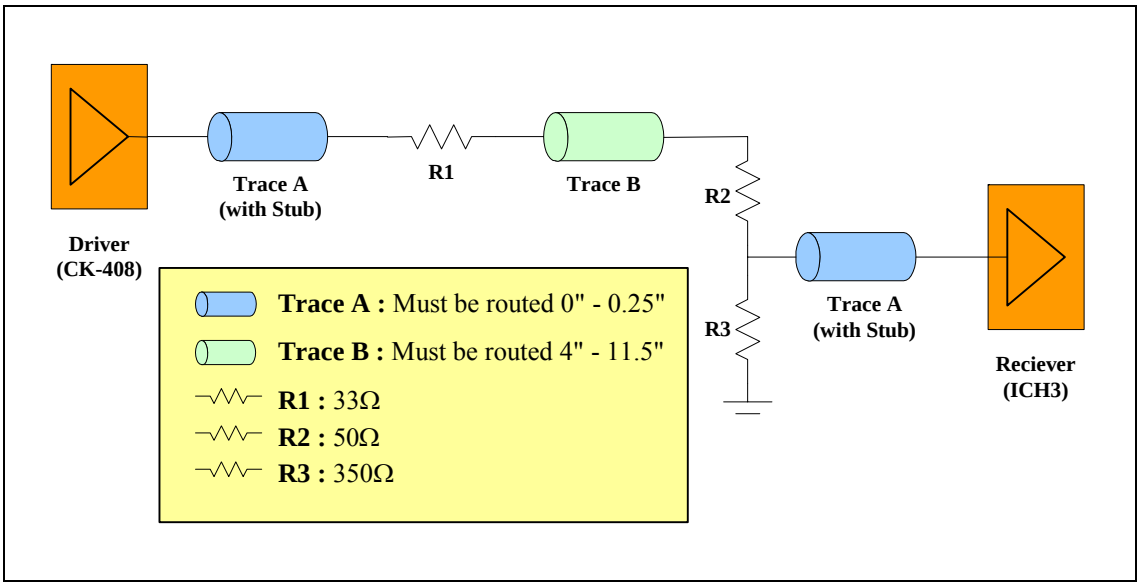
10.1.8.1. APIC_CLK at CPU

Figure 68. Topology for APIC_CLK With CPU as Receiver



10.1.8.2. APIC_CLK at ICH3-M

Figure 69. Topology for APIC_CLK with ICH3-M as Receiver



11. Intel 830 Chipset Family Power Delivery

The Intel 830 Chipset family platform supports the "Instantly Available PC Design Guidelines" via the *Suspend-to-RAM* (STR) state. During STR, only the necessary devices are powered. These devices include: main memory, the ICH3-M resume well, PCI wake devices (via 3.3 Vaux), AC'97 and optionally USB (USB can only be powered if sufficient standby power is available). To ensure that enough power is available during STR, a thorough power budget should be completed. The power requirements should include each device's power requirements, both in *suspend* and in *full-power*. The power requirements should be compared against the power budget supplied by the power supply. Due to the requirements of main memory and PCI 3.3 Vaux (and possibly other devices in the system), it is necessary to create a *dual* power rail.

The solutions given in this Design Guide are only examples. There are many power distribution methods that achieve the similar results. It is critical, when deviating from these examples to consider the effect of the change.

11.1. High Frequency Decoupling Design

11.1.1. Intel 830 Chipset Family GMCH-M Decoupling Guidelines

- 1.25 V core: 10x0.1 µF
- 1.2 V Vtt: 10x0.1 µF
- 1.5 V AGP/DVO: 10x0.1 µF
- 1.8 V CMOS RAC: 1x0.1 µF, 1x1 µF
- 1.8 V Hub Interface: 1x0.1 µF, 1x1 µF
- 3.3-V system memory: 5x0.1 µF
- 3.3-V GPIO: 5x0.1 µF

Table 44. GMCH-M Decoupling Capacitor Recommendation

Power	Decoupling Requirements
1.25 V core	Use 10 of 0.1 µF decoupling cap
1.2 V Vtt	Use 10 of 0.1 µF decoupling cap
1.5 V AGP/DVO	Use 10 of 0.1 µF decoupling cap
1.8 V CMOS RAC	Use 1 of 0.1 µF and 1 of 1 µF decoupling cap
1.8 V Hub Interface	Use 1 of 0.1 µF and 1 of 1 µF decoupling cap
3.3 V system memory	Use 5 of 0.1 µF decoupling cap
3.3 V GPIO	Use 5 of 0.1 µF decoupling cap

11.1.2. Intel 830 Chipset Family ICH3-M Decoupling Guidelines

The ICH3-M is capable of generating large current swings when switching between logic high and logic low. This condition could cause the component voltage rails to drop below specified limits. To avoid this type of situation, ensure that the appropriate amount of bulk capacitance is added in parallel to the voltage input pins. Intel recommends that the developer use the amount of decoupling capacitors specified in to ensure the component maintains stable supply voltages. The capacitors should be placed as close to the package as possible (200 mils nominal). Intel recommends that for prototype board designs the designer include pads for extra power plane decoupling caps.

Table 45. Decoupling Capacitor Recommendation

Power	Decoupling Requirements	Decoupling Placement
V_CPU_IO[2:0]	Use **1** 0.1 µF decoupling cap.	Locate within 100 mils of the ICH3-M CPU interface balls
Vcc3_3	Requires **6** 0.1 µF decoupling caps	• Distribute around the ICH3-M package sides within 100 mils from the package balls: Top near AUX/PCI Left across the PCI and LPC Bottom near IDE Right near LED drivers
VccSus3_3 (Includes LAN)	Requires **2** 0.1 µF decoupling cap.	• Place one cap on the tip side within 200 mils of the USB center • Bottom side near the Vccsus3_3 supply
Vcc1.8	Requires **4** 0.1 µF decoupling caps.	• Locate 2 caps distributed local to the Hub Interface; within 50 mils of the package HI balls • Distribute remaining cap(s) on the left and bottom sides of the package for core delivery
VccSus1.8 (Includes LAN)	Requires 1 0.1 µF decoupling cap.	• Locate within 200 mils of balls B23 and C23 of the ICH3-M
V5REF	Requires 1 0.1 µF decoupling cap. V5REF is the reference voltage for 5 V tolerant inputs in the ICH3-M. Tie to balls V5REF[2:1]. V5REF must be powered up before Vcc3_3, or after Vcc3_3 within 0.7 V. Also, V5REF must power down after Vcc3_3, or before Vcc3_3 within 0.7 V.	
V5REF_Sus	Requires 1 0.1 µF decoupling cap. V5REF_Sus is the reference voltage for some 5-V tolerant inputs in the Intel ICH3-M (USB data and over current signals). V5REF_Sus must be powered up before VccSus3_3, or after VccSus3_3 within 0.7 V. Also, V5REF_Sus must power down after VccSus3_3, or before VccSus3_3 within 0.7 V.	

Power Supply Ramp Considerations

11.1.3. GMCH-M/ICH3-M Platform Power-Up Sequence

The figure describes the power-on timing sequence for an Intel 830 Chipset family GMCH-M/ICH3-M based platform.

Figure 70. GMCH-M/ICH3-M Platform Power-up Sequence

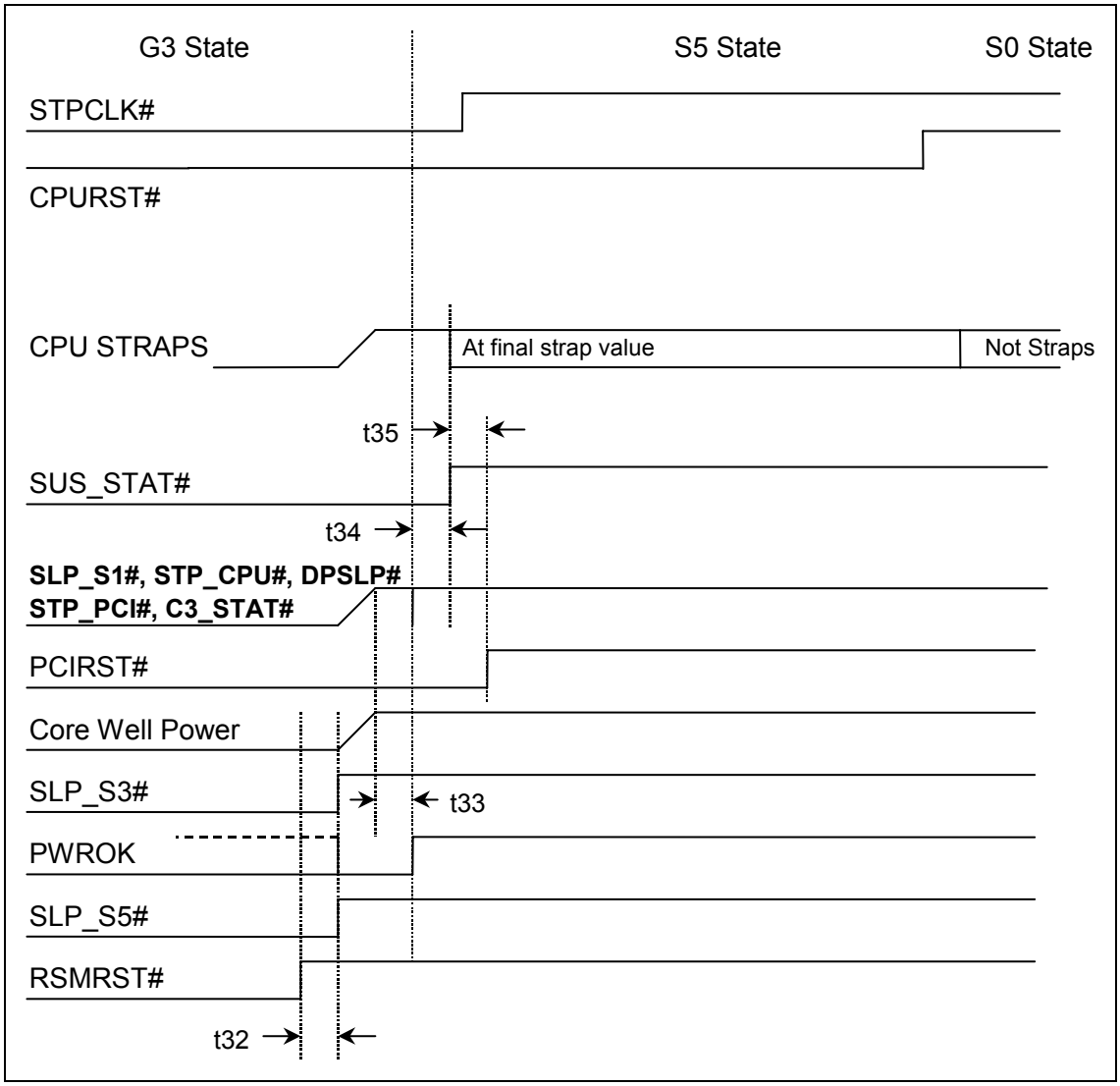


Table 46. Timing Sequence Parameters for Figure 70

Description	Min	Max	Units
T32 RSMRST# high to signals high	5	Infinity	ms
T33 Core well power stable to PWROK active	10		ms
T34 PWROK (and VRMPWRGD/VGATE) active to SUS_STAT# high and Frequency straps at appropriate value	32	34	RTC clock
T35 SUS_STAT# high to PCIRST# high	1	3	RTC clock

11.1.4. 1.8-V and 3.3-V Power Sequencing

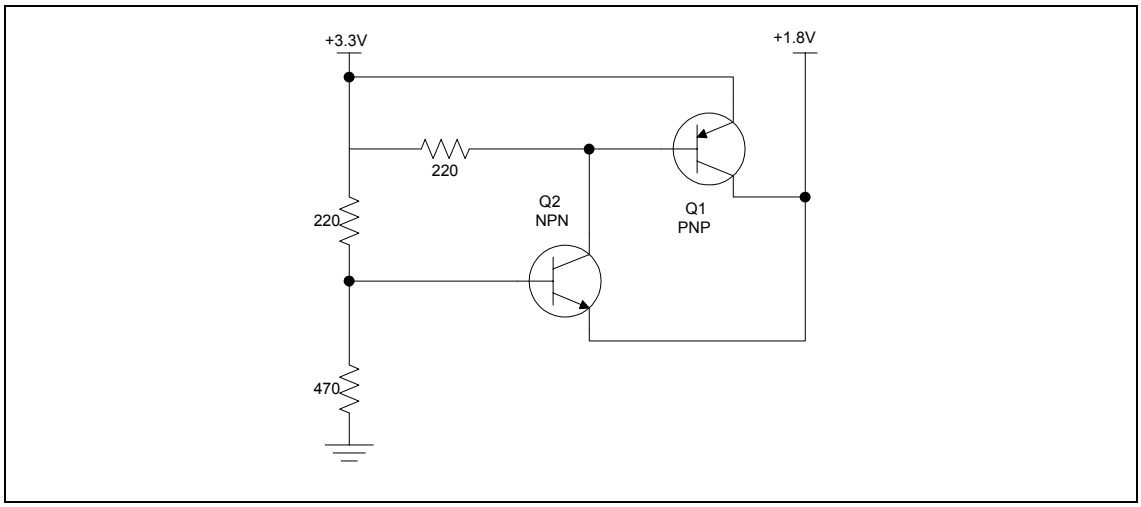
The ICH3-M has two pairs of associated 1.8-V and 3.3-V supplies. These are {V_{CC}1_8, V_{CC}3_3} and {V_{CC}Sus1_8, V_{CC}Sus3_3}. The ICH3-M has a third pair {V_{CC}LAN1_8, V_{CC}LAN3_3}. These pairs are assumed to power up and power down together. **The difference between the two associated supplies must never be greater than 2.0 V.** The 1.8- V supply may come up before the 3.3- V supply without violating this rule (though this is generally not practical in a desktop environment, since the 1.8- V supply is typically derived from the 3.3- V supply by means of a linear regulator).

One serious consequence of violation of this "2 V Rule" is electrical overstress of oxide layers, resulting in component damage.

The majority of the ICH3/ICH3-M I/O buffers are driven by the 3.3- V supplies, but are controlled by logic that is powered by the 1.8- V supplies. Thus, another consequence of faulty power sequencing arises if the 3.3- V supply comes up first. In this case, the I/O buffers will be in an undefined state until the 1.8-V logic is powered up. Some signals that are defined as "Input-only" actually have output buffers that are normally disabled, and the ICH3-M may unexpectedly drive these signals if the 3.3- V supply is active while the 1.8- V supply is not.

The figure below is an example power-on sequencing circuit that ensures the “2 V Rule” is obeyed. This circuit uses a NPN (Q2) and PNP (Q1) transistor to ensure the 1.8-V supply tracks the 3.3- V supply. The NPN transistor controls the current through PNP from the 3.3- V supply into the 1.8- V power plane by varying the voltage at the base of the PNP transistor. By connecting the emitter of the NPN transistor to the 1.8- V plane, current will not flow from the 3.3- V supply into 1.8- V plane when the 1.8- V plane reaches 1.8- V.

Figure 71. Example 1.8-V and 3.3-V Power Sequencing Circuit



When analyzing systems that may be "marginally compliant" to the 2-V Rule, please pay close attention to the behavior of the ICH3-M's RSMRST# and PWROK (also LAN_RST in ICH3-M) signals, since these signals control internal isolation logic between the various power planes:

- RSMRST# controls isolation between the RTC well and the Resume wells.
- PWROK controls isolation between the Resume wells and Main wells
- LAN_RST controls isolation between the LAN wells and the Resume wells (applies only to ICH3-M)

If one of these signals goes high while one of its associated power planes is active and the other is not, a leakage path will exist between the active and inactive power wells. This could result in high, possibly damaging, internal currents.

11.1.5. 3.3-V and V5REF Sequencing

V5REF is the reference voltage for 5-V tolerance on inputs to the ICH3-M. V5REF must be powered up before Vcc3_3, or after Vcc3_3 within 0.7 V. Also, V5REF must power down after Vcc3_3, or before Vcc3_3 within 0.7 V. The rule must be followed in order to ensure the safety of the ICH3. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the V_{CC}3_3 rail. Figure 72 shows a sample implementation of how to satisfy the V5REF and 3.3-V sequencing rule.

This rule also applies to the stand-by rails, but in most platforms, the V_{CC}Sus3_3 rail is derived from the V_{CC}Sus5 and therefore, the V_{CC}Sus3_3 rail will always come up after the V_{CC}Sus5 rail. As a result, V5REF_Sus will always be powered up before V_{CC}Sus3_3. In platforms that do not derive the V_{CC}Sus3_3 rail from the V_{CC}Sus5 rail, this rule must be comprehended in the platform design.

As an additional consideration to comply with USB 2.0 specification requirements regarding continuous short conditions, V5REF_Sus pins must be connected to 5 volts. 5VREF_Sus affects 5V tolerance for all USB signals, both over-current and data pins. USB 2.0 specification requires that USB controller to withstand a continuous short between the USB 5-V connector supply to a USB signal at the connector for 24hrs. Figure 72 and Figure 73 provide options for connecting V5REF_Sus to 5 V on mobile

platforms. Figure 72 is for platforms that support +V5_Always (5V always ON). Figure 73 represents a connection to V5REF_Sus for platforms that do not support +V5_Always.

Figure 72. Example 3.3-V and V5REF Sequencing Circuitry

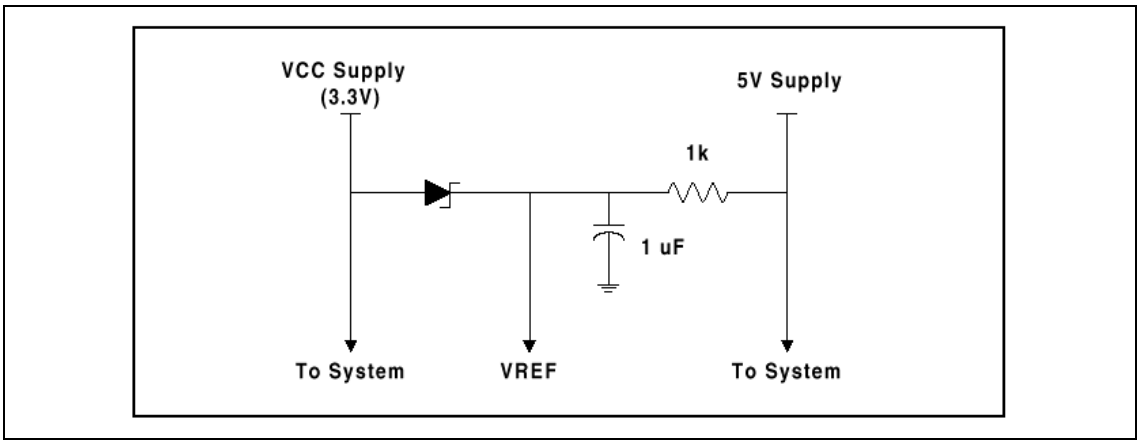


Figure 73. V5REF_Sus Option 1: +V5_Always Available in Platform

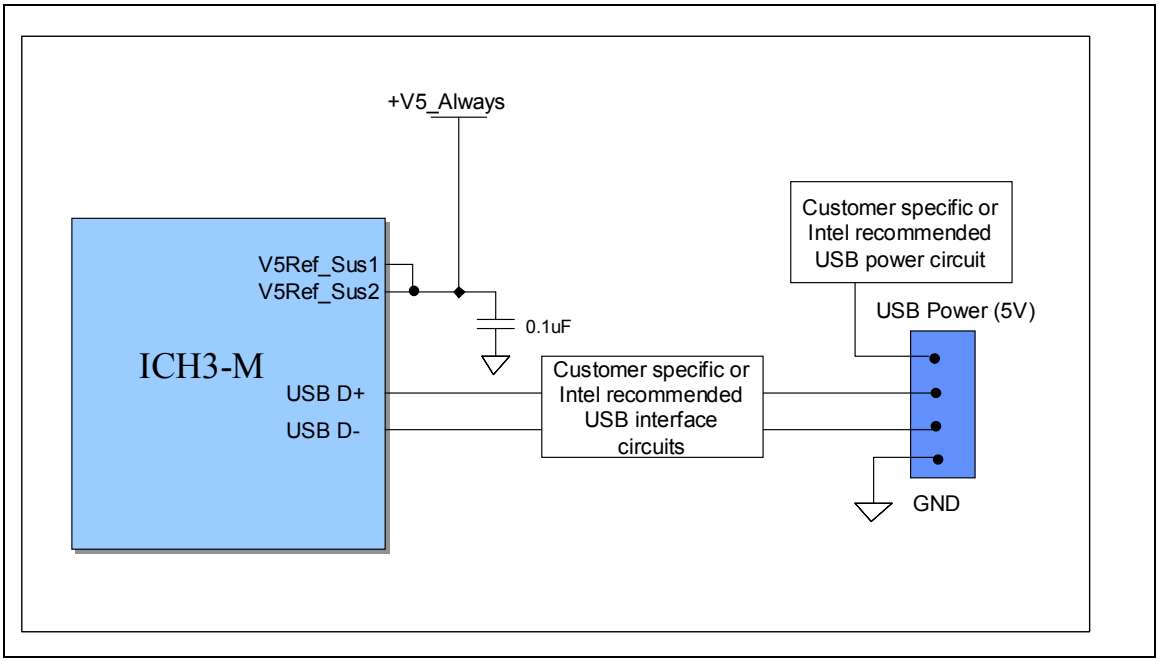
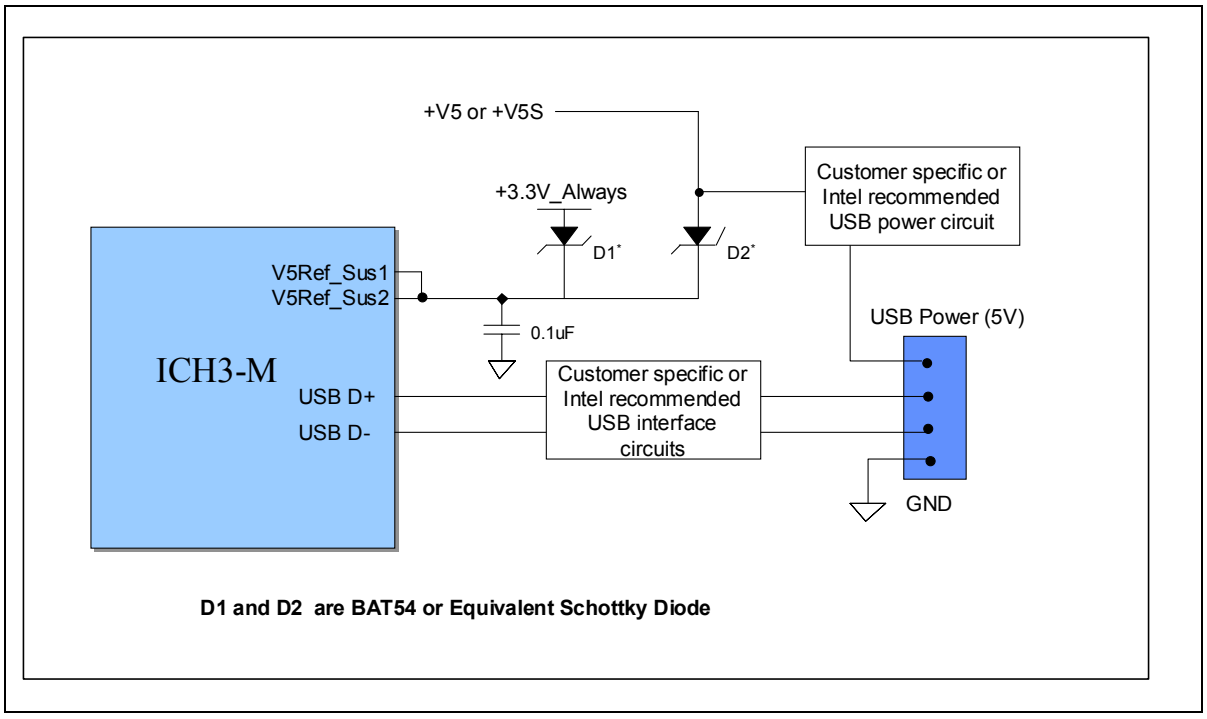


Figure 74. V5REF_Sus Option 1: +V5_Always Not Available in Platform



11.1.6. 3.3-V and 1.25-V Power Sequencing Requirement

There are nine balls powered up by the Vcc GPIO 3.3-V supply. If the 3.3-V (Vcc GPIO) rail is powered on before the 1.25-V rail during a cold boot, this will put the core predriver to the 3.3-V rails into an unknown stage resulting in high temperature and leakage through the balls. The 1.25-V rails must be powered on within 200 ms of the 3.3-V rails. To ensure proper operation, the GPIO pairs (6 signals) must be pulled up to the 3-V non-switched rail. Otherwise, the pull up resistors for the GPIO pairs can remain on the 3-V switched rail assuming the 1.25-V rail is powered on simultaneously to the 3.3-V rail

11.1.7. 1.25-V and 1.8-V Power Sequencing

In addition the Intel 830 Chipset family GMCH-M has a 1.25-V and 1.8-V supplies. These pairs are assumed to power up and power down together also. **The difference between the two associated supplies must never be greater than 1.5 V.** The 1.25-V supply may come up before the 1.8-V supply without violating this rule (though this is generally not practical in a mobile environment, since the 1.25-V supply is typically derived from the 1.8-V supply by means of a linear regulator). The above power circuit could be used as an example for the 1.25-V to 1.8-V sequencing.

11.2. ICH3-M (Mobile) Power Consumption Numbers

The following table shows the preliminary ICH3-M power consumption estimates.

Table 47. ICH3-M (With Mobile Planes) Maximum Power Consumption

Power Plane	Max Power Consumption				
	S0	S1M	S3	S4/S5	G3
1.8 V Core	550 mA	20 mA	N/A	N/A	N/A
3.3 V I/O	420 mA	0.5 mA	N/A	N/A	N/A
1.8 V LAN	30 mA	6 mA	1 mA	1 mA	N/A
3.3 V LAN	12 mA	6 mA	4 mA	4 mA	N/A
1.8 V SUS	64 mA	7.5 mA	7.5 mA	7.5 mA	N/A
3.3 V SUS	14 mA	.05 mA	.05 mA	.05 mA	N/A
VccRTC	N/A	N/A	N/A	N/A	4 µA

- Both 1.8LAN and 3.3LAN S0 max were measured with LAN 100 Mbs full duplex test.
- LAN measurements represent ICH3-M power only; they do not include PHY.
- 1.8LAN and 3.3LAN were connected to 1.8Stby and 3.3Stby, respectively.
- 3.3LAN with no PHY connected is 0.01 mA; 1.8LAN with no PHY is 0 mA.
- 3.3-V SUS S0 was measured with USB traffic (6 ports populated at Full speed).

11.3. Thermal Design Power

The thermal design power is the estimated maximum possible expected power generated in a component by a realistic application. It is based on extrapolations in both hardware and software technology over the life of the product. It does not represent the expected power generated by a power virus. The thermal design power numbers for the ICH3-M are listed in Table 48.

Table 48. ICH3-M Component Thermal Design Power

ICH3-M - Thermal Design Power Consumption Dissipation (Estimated)	
ICH3-M	2 W (maximum)

11.4. Intel 830 Chipset Family GMCH-M TDP Characteristics

Table 49. GMCH-M TDP Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
$TDP_{Typ(dis)}$	133 MHz PSB, 2 PC133 SO-DIMMs (Discrete)			W	1,3 (IGD* disabled)
$TDP_{Typ(UMA)}$	133 MHz PSB, 2 PC133 SO-DIMMs (UMA)		3.8	W	1,2,3 (166 MHz core)
$TDP_{Typ(LM)}$	133 MHz PSB, 2 PC133 SO-DIMMs (LM)		3.5	W	1,2,3 (166 MHz core)
$TDP_{Max(dis)}$	133 MHz PSB, 2 PC133 SO-DIMMs (Discrete)		6.5	W	4,5 (IGD disabled)
$TDP_{Max(UMA)}$	133 MHz PSB, 2 PC133 SO-DIMMs (UMA)		7.4	W	4,5 (166 MHz core)
$TDP_{Max(LM)}$	133 MHz PSB, 2 PC133 SO-DIMMs (LM)		7.7	W	4,5 (166 MHz core)

IGD= Integrated Graphics Device

NOTES:

1. The Thermal Design Power (typical) or TDP_{Typ}, is a recommendation based on average and sustainable peak power dissipation of publicly available applications under normal operating conditions, at nominal Vcc, and worst-case temperature. The derivation and calculation of this specification is based on the characterization of a variety of real applications.
2. The TDP_{Typ} was measured on pre-production silicon. Therefore, it is subject to change.
3. The TDP_{Typ} was estimated based on the configurations listed. TDP_{Typ} is the recommended design power.
4. The Thermal Design Power (maximum) or TDP_{Max}, is a recommendation based on the maximum power dissipated under normal operating conditions, at nominal Vcc, under worst-case temperature, and executing the worst case instruction mix. Worst-case instruction mix refers to the code sequence that results in the highest sustainable total simultaneous power dissipated within the die silicon, from all power supplies.
5. The TDP_{Max} was estimated based on the configurations listed.

11.5. Pullup and Pulldown Resistor Values

Pullup and pulldown values are system dependent. The appropriate value for your system can be determined from an AC/DC analysis of the pullup voltage used, the current drive capability of the output driver, input leakage currents of all devices on the signal net, the pullup voltage tolerance, the pullup/pulldown resistor tolerance, the input high/low voltage specifications, the input timing specifications (RC rise time), etc. Analysis should be done to determine the minimum/maximum values that may be used on an individual signal. Engineering judgment should be used to determine the optimal value. This determination can include cost concerns, commonality considerations, manufacturing issues, specifications, and other considerations.

Equation 4. Min/Max Pullup/Pulldown Resistor Values

A simplistic DC calculation for a pullup value is:

$$R_{MAX} = (Vcc_{PU}\,MIN - V_{IH}\,MIN) / I_{LEAKAGE}\,MAX$$

$$R_{MIN} = (Vcc_{PU}\,MAX - V_{IL}\,MAX) / I_{OL}\,MAX$$

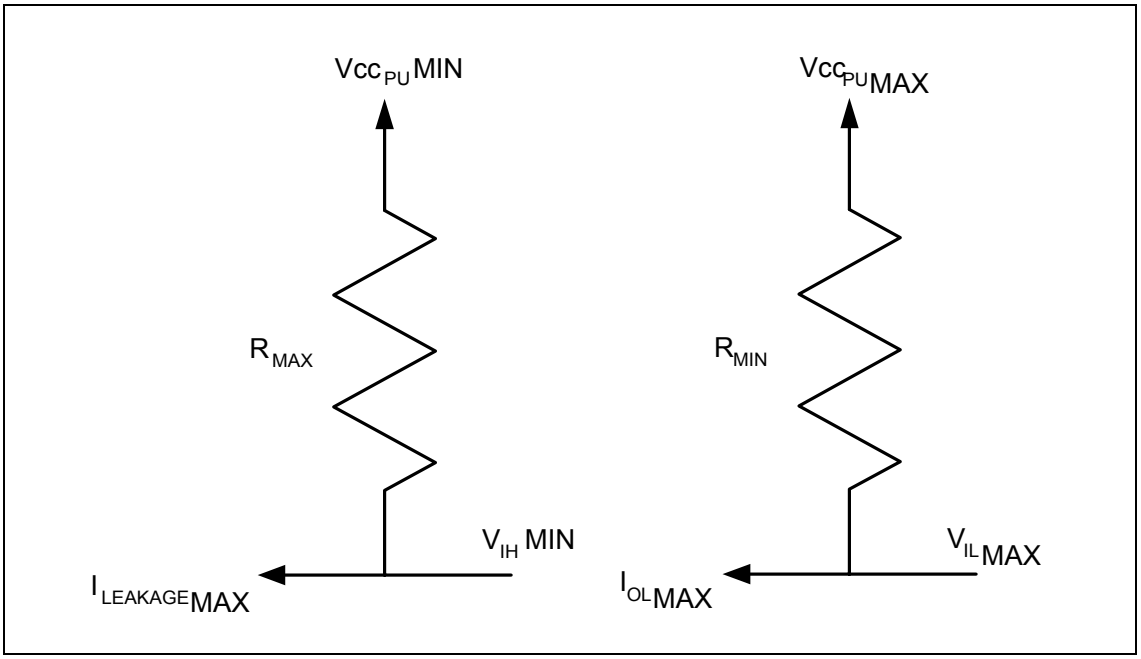
Since $I_{LEAKAGE}$ MAX is normally very small, R_{MAX} may not be meaningful. R_{MAX} is also determined by the maximum allowable rise time. The following calculation allows for t (the maximum allowable rise

time) and C (the total load capacitance in the circuit, including input capacitance of the devices to be driven) output capacitance of the driver, and line capacitance. This calculation yields the largest pullup resistor allowable to meet the rise time t.

Equation 5. R_{MAX} for Maximum Allowable Rise Time

$$R_{MAX} = -t / (C * In(1-(V_{IH}\,MIN / Vcc_{PU}\,MIN)))$$

Figure 75. Pullup Resistor Example



11.6. Power Supply PWRGOOD Requirements

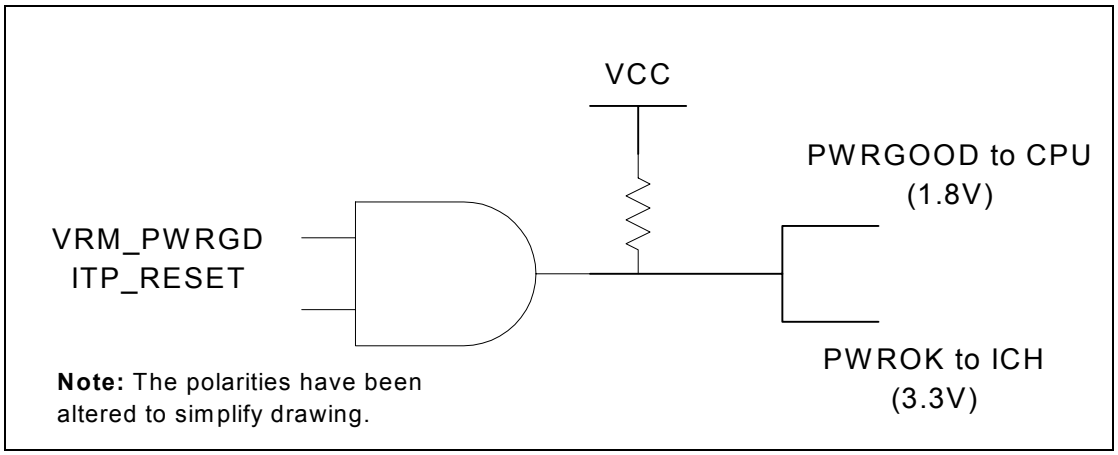
The PWROK signal must be glitch free for proper power management operation. The ICH3-M sets the PWROK_FLR bit (ICH GEN_PMCON_2, General PM Configuration 2 Register, PM-dev31: function 0, bit 0, at Offset A2h). If this bit is set upon resume from S3 power down, the system will reboot, and control of the system will not be given to the program running when entering the S3 state. System designers should ensure that PWROK signal designs are error free.

11.7. Power Management Signals

- A power button is required by the ACPI specification.
- PWRBTN# is connected to the front panel on/off power button. The ICH3-M integrates 16 msec debouncing logic on this pin.
- AC power loss circuitry has been integrated into the ICH3-M to detect power failure.
- Intel recommends that the PS_POK signal from the power supply connector be routed through a Schmitt trigger to square-off and maintain its signal integrity, and not be connected directly to logic on the board.
- PS_POK logic from the power supply connector can be powered from the core voltage supply.

- RSMRST# logic should be powered by a standby supply, making sure that the input to the ICH3-M is at a 3-V level. The RSMST# signal requires a minimum time delay of 1 millisecond from the rising edge of the standby power supply voltage. A Schmitt trigger circuit is recommended to drive the RSMRST# signal. To provide the required rise time, the 1-ms delay should be placed before the Schmitt trigger circuit. The reference design implements a 20-ms delay at the input of the Schmitt trigger to ensure the Schmitt trigger inverters have sufficiently powered up before switching the input. Also ensure that voltage on RSMRST# does not exceed VCC(RTC).
- Intel recommends that 3.3-V logic be used to drive RSMRST# to alleviate rise time problems when using a resistor divider from VCC5.
- The PWROK signal to the chipset is a 3-V signal.
- The core well power valid to PWROK asserted at the chipset is a minimum of 1 msec.
- PWROK to the chipset must be deasserted after RSMRST#.
- PWRGOOD signal to CPU is driven with an open collector buffer pulled up to 1.8 V using a 330-Ω resistor.
- The circuitry checks for both CPU VRM powered up, and the PS_POK signal from the power supply connector before asserting PWRGOOD and PWROK to the CPU and the ICH3-M.

Figure 76. PWRGOOD and PWROK Logic



- RI# can be connected to the serial port if this feature is used. To implement ring indicate as a wake event, the RS232 transceiver driving the RI# signal must be powered when the ICH3-M suspend well is powered. This can be achieved with a serial port transceiver powered from the standby well that implements a shutdown feature.

11.7.1. Power Button Implementation

The items below should be considered when implementing a power management model for a mobile system. The power states are as follows:

- S1M – Power On Suspend
- S3 - STR (Suspend To RAM)
- S4 - STD (Suspend To Disk)
- S5 - Soft-off
- Wake: Pressing the power button wakes the computer from S1M-S5.
- Sleep: Pressing the power button signals software/firmware in the following manner:
  - If SCI is enabled, the power button will generate an SCI to the OS. The OS will implement the power button policy to allow orderly shutdowns. Do not override this with additional hardware.
- If SCI is not enabled:
  - Enable the power button to generate an SMI and go directly to soft-off or a supported sleep state.
  - Poll the power button status bit during POST while SMIs are not loaded and go directly to soft-off if it gets set.
  - Always install an SMI handler for the power button that operates until ACPI is enabled.
- Emergency Override: Pressing the power button for 4 seconds goes directly to S5.
  - This is only to be used in EMERGENCIES when system is not responding.
  - This will cause the user data to be lost in most cases.
- Do not promote pressing the power button for 4 seconds as the normal mechanism to power the machine off - this violates ACPI.
- To be compliant with the latest PC9x specification, machines must appear off to the user when in the S1M-S4 sleeping states. This includes:
  - All lights except a power state light must be off.
  - The system must be inaudible: silent or stopped fan; drives are off.
- When entering S1M, CPU should be put into Deep Sleep (C3) thorugh one of the following ways:
  - Stop the host clock to CPU
  - Assert CPU DPSLP# pin

Note: Contact Microsoft* for the latest information concerning PC9x and PC01 and Microsoft Logo programs.

11.8. ACPI 2.0 Support

Advanced Configuration and Power Management Interface (ACPI) primarily describes and runs motherboard devices. ACPI is completely controlled by the operating system that OS drivers directly power down PCI/AGP devices. However, system or SMI BIOS plays a part of waking the system. Device drivers save and restore state while bus drivers change the physical power state of the device.

The Intel 830 Chipset family GMCH-M power management architecture is designed to allow single systems to support multiple suspend modes and to switch between those modes as required. A suspended system can be resumed via a number of different events. The system returns to full operation

where it can continue processing or be placed into another suspend mode (potentially a lower power mode than it resumed from).

The GMCH-M supports the minimum requirements for ACPI support. The GMCH-M must support the minimum requirements for both system logic and for graphics controllers, as well as be capable of controlling monitors minimum functions. The transition sequences of entering and exiting system, CPU, and graphics states are described in respective sections below.

11.8.1. Intel 830 Chipset Family System and CPU States

Table 50 shows the state combinations that Intel 830 Chipset Family supports.

Table 50. Intel 830 Chipset Family Platform ACPI System and CPU States

Global (G) State	Sleep (S) State	Processor State	Description
G0	S0	Full On (C0)	Full On
G0	S0	Auto-Halt (C1)	Auto Halt
G0	S0	Quick Start (M) (C2)	Quick Start
G0	S0	Deep Sleep (C3) / Deeper Sleep	Deep Sleep/Deeper Sleep
G1	S1M	Deep Sleep (C3) /Deeper Sleep	Power On Suspend (POS)
G1	S3	Power off	Suspend to RAM (STR)
G1	S4	Power off	Suspend to Disk (STD/Hibernate)
G2	S5	Power off	Hard Off.
G3	NA	Power off	Mechanical Off.

11.8.2. Intel 830MP Chipset ACPI States Supported

Intel 830MP Chipset supports the following ACPI States:

1. System States
   a. G0/S0 Full On
   b. G1/S1M Power On Suspend (POS). System Context Preserved.
   c. G1/S3 Suspend to RAM (STR). Power and context lost to chipset.
   d. G1/S4 Suspend to Disk (STD). All power lost (except wakeup on ICH3-M)
   e. G2/S5 Hard off. Total reboot.
2. CPU States
   a. C0 Full On
   b. C1 Auto Halt
   c. C2 Mobile Quick Start (lower power than Stop Grant).
   d. C3 Deep Sleep. Clock to CPU stopped.

11.8.3. Intel 830M and 830MG Chipset ACPI States Supported

Intel 830M and 830MG Chipset supports the following ACPI States:

1. System States
   a. G0/S0 Full On
   b. G1/S1M Power On Suspend (POS). System Context Preserved.
   c. G1/S3 Suspend to RAM (STR). Power and context lost to chipset.
   d. G1/S4 Suspend to Disk (STD). All power lost (except wakeup on ICH3-M)
   e. G2/S5 Hard off. Total reboot.
2. CPU States
   a. C0 Full On
   b. C1 Auto Halt
   c. C2 Mobile Quick Start (lower power than Stop Grant).
   d. C3 Deep Sleep. Clock to CPU stopped.
3. Internal Graphics Device state
   a. D0 On
   b. D1 Standby
   c. D3 Hot (S1 state)
   d. D3 Cold (S3 state)

11.8.4. Intel 830M and 830MG Graphics Device Power Management Requirements

For ACPI 2.0 compliance, the IGD internal graphics controller is required to support the ACPI D0, D2, and D3 device states. For the ACPI D3 device power state, it is possible for IGD controller to support either a D3 HOT or D3 COLD state given certain restrictions. The D3 HOT state is only supported in the S1M state, while the D3 COLD state is implemented in the S3 state. Although the ACPI 2.0 specification does not define nor differentiate between D3 HOT and D3 COLD, the Intel 830M and 830MG Chipset has special requirements for D3 HOT and COLD implementations.

11.8.4.1. AGP_BUSY# requirements for IGD interface

The GMCH-M AGP_BUSY# signals allows power management signaling between the graphics controller and the ICH3-M. AGP_BUSY# indicates that the graphics device is busy. AGP_BUSY# (ICH3-M signal) is directly connected to the Intel 830M and 830MG GMCH-M AGPBUSY# signal. For proper implementation, please consult Intel Field Application Engineers.

The Intel 830M and 830MG AGP_BUSY# 3.3-V signal should be pulled up to 3-V switched rail, the power rail that is powered OFF during S3.

11.8.5. 830M and 830MG Internal Graphics DPMS Monitor ‘D’ States Support

The monitor is considered a child device of the graphics controller. Its ACPI states are controlled through the graphics controller. DPMS (Display Power Management Signaling) is a VESA (Video Electronics Standards Association) specification that provides a method for the graphics controller to put the monitor in a particular power management state by controlling the presence or absence of pulses on

the HSYNC and VSYNC signals. The D state of the monitor can be set independently of the graphics controller, but will always be equal to or higher (in number, lower in power) than the graphics controller. The monitor is considered a "child device" to the graphics controller. Table 51 lists each combination. DPMS defines these states as ON, Standby, Suspend, and OFF, but they are mapped into the ACPI D0 to D3 states.

The D state of the monitor can be set independently of the graphics controller, but will always be equal to or higher (in number, lower in power) than the graphics controller. The monitor is considered a "child device" to the graphics controller.

Table 51. Combinations of Monitor and Graphics Power Down States for 830M and 830MG

Graphics Controller	Monitor State	HSYNC/VSYNC Status
D0	D0 = On	Pulse HSYNC and VSYNC
D0	D1 = Standby	Pulse VSYNC
D0	D2 = Suspend	Pulse HSYNC
D0	D3 = Off	No pulse on HSYNC and VSYNC
D1*	D1*	Pulse VSYNC
D1*	D2*	Pulse HSYNC
D1	D3	No pulse on HSYNC and VSYNC
D3	D3	No pulse on HSYNC and VSYNC

NOTE: *Requires DPMS clock circuitry. See Figure 77.

In D1 the graphics controller must be able to toggle either HSYNC or VSYNC, depending on the monitor mode. In D2 the graphics device must be able to toggle HSYNC. The pulses must be at least 10 kHz for HSYNC and 40 Hz for VSYNC.

11.8.6. Intel 830M and 830MG Chipset Internal Graphics "D" states

PC9x implies that D0 and D3 are obligatory for graphics controllers. D0, D2, and D3 are obligatory for monitors. The Intel 830M and 830MG Chipset GMCH-M also implements D1 for the graphics controller and monitors. System SDRAM state is generally controlled by S-States and C-States rather than D-States. With internal graphics the system SDRAM will remain available when the CPU is in C3.

11.8.6.1. D0 Graphics Adapter State – Active State

In the D0 Power State, everything is operating. This is the normal ON State for the ICD graphics functions. The Intel 830M and 830MG Chipset GMCH-M graphics functions enter this state out of power-on-reset.

11.8.6.2. The D1 Graphics Adapter State

In the D1 Power State, the graphics must go to a lower power state. The displays are blank, but memory and registers must be maintained. The emphasis is on a fast recovery in this mode.

11.8.6.3. The D3 Graphics Adapter State

The D3 Power State is the lowest power mode. Displays are off, and the registers and memory need not be maintained. The PCI configuration space must be accessible, in order to write the power state back to D0. If S1M /D3 state combination support required; the DPMS_CLK circuitry must be implemented. Please refer to Section 11.9.6.

In response to a command to enter D3, the IGD will disable the memory and IO space, all clocks that are not required for accessing graphics configuration space, interrupts, and the DAC outputs. Bus master accesses are disabled and the graphics core will be in RESET. The HSYNC and VSYNC outputs do not toggle in this state.

When the OS decides to put the IGD graphics functions into D3 power state, it calls the IGD graphics driver so that the driver saves the device context. Device context consists of the IGD graphics mode as well as local and non-local video memory context. External parts context must also be stored.

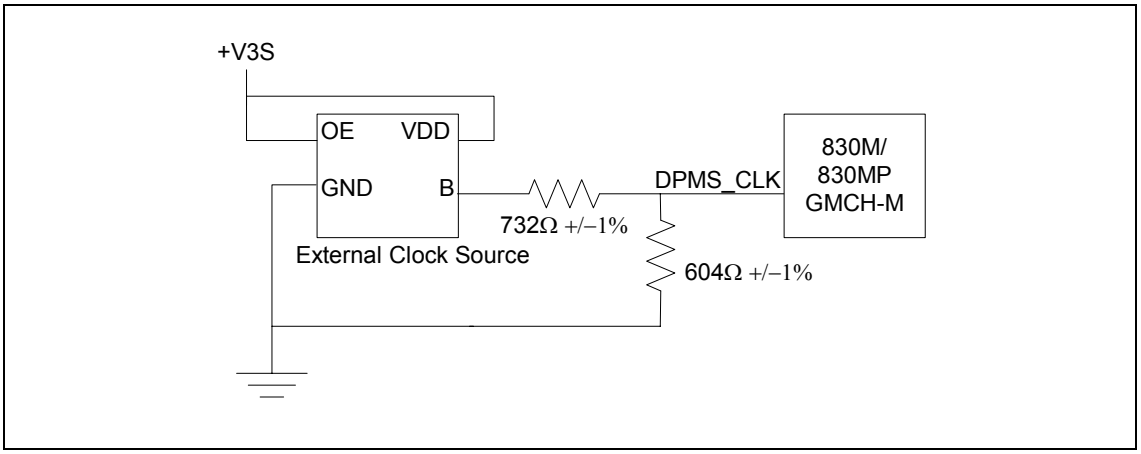
During exit from the D3 COLD, configuration registers must be restored before PCI enumeration and driver access occurs.

11.8.7. Intel 830M and 830MG Chipset DPMS Clock Signaling in D1/S1 State

When the Intel 830M and 830MG Chipset GMCH-M graphics controller is in the Mobile S1 State, the graphics core clock and dot clocks are stopped, causing HSYNC and VSYNC generation to stop. If the system is configured to allow the graphics controller to be in D1 while the system is in Mobile S1, all clocks in the system, including the clock generator chip are shut off. Potentially the only clock running is the 32 kHz of the Real Time Clock.

For Mobile D1/S1 support requires an external clock source. The DPMS_CLK signal provides the clock source needed to generate pulses on HSYNC and VSYNC signals in D1/S1 state. The DPMS_CLK signal is muxed with GAD30 provides the clock source to generate pulses on HSYNC and VSYNC in the D1 State. The DMPS spec requirement is that HSYNC be at least 10 kHz when running and VSYNC be at least 40 Hz. The DPMS_CLK signal requires an external clock source, which may be either 32 kHz or a 33/66 MHz clock.

Figure 77. DPMS Support



11.8.8. AGP Busy/Stop Protocol With Internal Graphics Revision

The AGP_BUSY# and STP_AGP# signals allow power management signaling between an external AGP graphics controller and the ICH3-M. AGP_BUSY# indicates that the AGP device is busy. C3_STAT# (STP_AGP#) is the signal, which used for indicating to the AGP device that a C3 state transition is beginning or ending. AGP_BUSY# (ICH3-M signal) and STP_AGP# (AGP graphics controller signal) are not directly connected to the Intel 830MP/830M Chipset GMCH-M. For proper implementations, please consult Intel Field Application Engineers.

12. System Design Checklist

The following checklist provides design recommendations and guidance for the Intel Mobile Pentium III Processor-M Processor systems with 133-MHz SDRAM memory subsystems based on the Intel 830 chipset. The checklist can be used to ensure all design recommendations in the 830 Chipset Family Design Guide have been followed during schematic and layout design reviews. However, this is not a complete list and does not guarantee that a design will function properly.

Please note, unless otherwise specified the default tolerance on resistors is ±5%. Please refer to Section 1.1 for reference documents.

12.1. Mobile Intel Pentium III Processor-M / Mobile Intel Celeron Processor

12.1.1. Resistor Recommendations

Mobile Intel Pentium III Processor-M / Mobile Intel Celeron Processor – Resistor Recommendations				
Signal	**System Pull-up/Pull-down**	**Ω**	**Notes**	**✓**
(pin) A2			Micro-FCBGA: Ball is NC Micro-FCPGA: Key is depopulated	
A[35:3]#	See Notes		A[35:3]# are connected to A[31:3]# on GMCH-M A[35:32]# are not supported by the chipset. Leave unconnected (NC).	
A20M#, DPSLP#, IGNNE#, INIT#, INTR/LINT0, NMI/LINT1, SMI#, STPCLK#			Pull-up resistors not required if using ICH3-M where signals are actively driven.	
BREQ0#	Pull-down to GND	10 Ω	Pull-down is alternative to having central agent driving BREQ0# low at reset.	
BSEL[1:0]	Pull-up to Vcc3_3	1 KΩ	See Intel® 830 Chipset Family Design Guide Sec 3.4	
EDGECTRLP	Pull-down to GND	110 Ω ± 1%		
FERR#	Pull-up to Vcc1_5	1.5 KΩ		
FLUSH#	Pull-up to Vcc1_5	3 KΩ		
GHI#			Has an integrated pull-up to VTT.	
IERR#	Pull-up to Vcc1_5	1.5 KΩ	Required pull-up for noise reduction.	
NCTRL	Pull-up to VTT	14 Ω ±1%		
PICCLK	See Sec 5.1, PCIF1 for topology info		**If the APIC is not used:** Disable IOAPIC in BIOS by setting MSR Offset: 1Bh, bit 11 (0 = disable) and using the configuration in Fig 86 or Fig 87. See “APICCLK” in Sec 12.6.1 for details. See Intel 830M Family CRB Sch. p7 or Fig 86	
PICD[1:0]	See Sec 8.1,		**If the APIC is not used:**	

Mobile Intel Pentium III Processor-M / Mobile Intel Celeron Processor – Resistor Recommendations				
Signal	**System Pull-up/Pull-down**	**Ω**	**Notes**	**✓**
	APICD[1:0] for topology info		See recommendations for PICCLK. See Intel 830M Family CRB Sch. p7 or Fig 86	
PWRGOOD	Pull-up to Vcc1_8	1.5 KΩ		
RESET#	Pull-up to VTT	56.2 Ω ±1%	Place resistor < 0.1" from CPU interface. Required pull-up for termination.	
RTTIMPEDP	Pull-down to GND	56.2 Ω ±1%		
TESTHI	Pull-up to VTT	1 KΩ	There are 2 TESTHI signals.[Ball E2 and Ball AF11]	
TESTLO	Pull-down to GND	1 KΩ	There are 2 TESTLO signals. [Ball Y4 and Ball M1]	
VID[4:0]	Pull-up to Vcc3_3	1 KΩ	Use 1 KΩ for reduced leakage. Intel 830M Family CRB Sch. uses 10 KΩ. See p4	
VTTPWRGD	Pull-up to VTT	1 KΩ	See Intel 830M Family CRB Sch. p7	
VCC[81:61,59:0]	Pull-up to VCC		81 VCC pins	
VCCT[37:0]	Pull-up to VTT		38 VCCT pins	
VSS[145:0]	Tie to GND		146 VSS pins	

NOTE: Default tolerance for resistors is ±5% unless otherwise specified.

12.1.2. In Target Probe (ITP)

Mobile Intel Pentium III Processor-M / Mobile Intel Celeron Processor– ITP					
Signal	**System Pull-up/Pull-down**	**Ω**	**Series Damping**	**Notes**	**✓**
DBINST#	Pull-up to VTT	10 KΩ			
DBRESET#	Pull-up to VccSus3_3	240 Ω			
POWERON	Pull-up to VTT	1.5 KΩ			
PRDY0#	Pull-up to VTT	56.2 Ω ±1%	240Ω	Place resistor < 1 inch from port. Debug port must be at end of trace.	
PREQ0#	Pull-up to Vcc1_5	200 Ω – 300 Ω		Resistor range is 200 Ω-300 Ω. Intel 830M Family CRB Sch. uses 200 Ω. See p6	
RESET#	Pull-up to VTT	56.2 Ω ±1%	240Ω	Place resistor < 1" from port. Debug port must be at end of trace.	
TCK	Pull-down to GND	39 Ω		Place resistor < 1" from port. Debug port must be at end of trace.	
TDI	Pull-up to Vcc1_5	200 Ω – 300 Ω		Resistor range is 200 Ω-300 Ω. Intel 830M Family CRB Sch. uses 200 Ω. See p6	
TDO	Pull-up to Vcc1_5	150 Ω			
TMS	Pull-up to Vcc1_5	39 Ω		Place resistor < 1" from port. Debug port must be at end of trace.	
TRST#	Pull-down to GND	510 Ω		If ITP/TAP unused, use 1.5 KΩ pull-down.	

12.1.3. Thermal Sensor

Mobile Intel Pentium III Processor-M / Mobile Intel Celeron Processor– Thermal Sensor				
Signal	**System Pull-up/Pull-down**	**Ω**	**Notes**	**✓**
ADD[1:0]	Pull-up to Vcc3_3	1 KΩ		
ALERT#	Pull-up to Vcc3_3	10 KΩ	To enable alert, ALERT# can be connected to THRM# on ICH3-M.	
DXN, DXP			Connect with 2200 pF crossover capacitor and route both signals on same layer.	
SMBCLK	Pull-up to Vcc3_3	10 KΩ		
SMBDATA	Pull-up to Vcc3_3	10 KΩ		
STBY#	Pull-up to Vcc3_3	10 KΩ		
VCC	See Notes		One 0.1 µF decoupling cap.	

12.1.4. PLL[2:1] RLC Filter

Mobile Intel Pentium III Processor-M / Mobile Intel Celeron Processor– PLL[2:1] RLC Filter			
Device	**Value**	**Notes**	**✓**
R	0 Ω	Total series resistance from VTT to top plate of cap must be > 0.35 Ω (2 Ω max) and depends on DCR_{max} of L and trace impedance used.	
L	4.7 µH		
C	33 µF_16 V		

12.1.5. Decoupling Recommendations

Mobile Intel Pentium III Processor-M / Mobile Intel Celeron Processor – High Frequency Decoupling Recommendations[1]					
Signal	**Configuration**	**F**	**Qty**	**Notes**	**✓**
CMOSREF[1:0]	Pull-down to GND	0.1 µF	2	Place near CPU. See Figure 77	
VCC	Underneath balls on solder side. On the peripheral near balls.	0.22 µF 10 µF_ 6.3 V	24 10	Use 2-3 vias per pad for reduced inductance during layout. Placement should be near processor for all.	
VREF[7:0]	Place within 500 mils of pins.	0.1 µF	3	Place near CPU. See Figure 76	
VTT	Place close to processor for all.	1 µF	10	Use 2 vias per pad for reduced inductance during layout.	

12.1.6. Reference Voltage Dividers

Mobile Intel Pentium III Processor-M / Mobile Intel Celeron Processor – Reference Voltage Dividers[1]				
Signal	**System Pull-up/Pull-down**	**Ω**	**Notes**	**✓**
VREF[7:0]	Voltage divider with decoupling caps	1 KΩ (top) 2 KΩ (bottom)	Shared node at [2/3]*VTT. See Section 12.2.5 for decoupling. See Intel 830M Family CRB Sch. p4 or Figure 76. Place voltage divider between CPU and GMCH-M w/ decoupling capacitors near CPU.	
CMOSREF[1:0]	Voltage divider with decoupling caps	0.5 KΩ (top) 1 KΩ (bottom)	Shared node at 1.00 V. See Sec 4.5 for decoupling. See Intel 830M Family CRB Sch. p4 or Figure 77. Place decoupling capacitors near CPU.	

NOTE: [1]All decoupling guidelines are recommendations based on our reference board design. Customers will need to take their layout & PCB board design into consideration when deciding on their overall decoupling solution.

Figure 78. GTL Reference Voltage

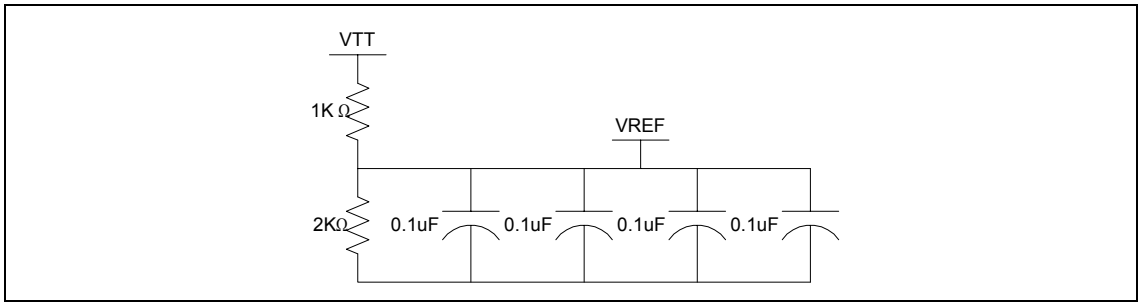
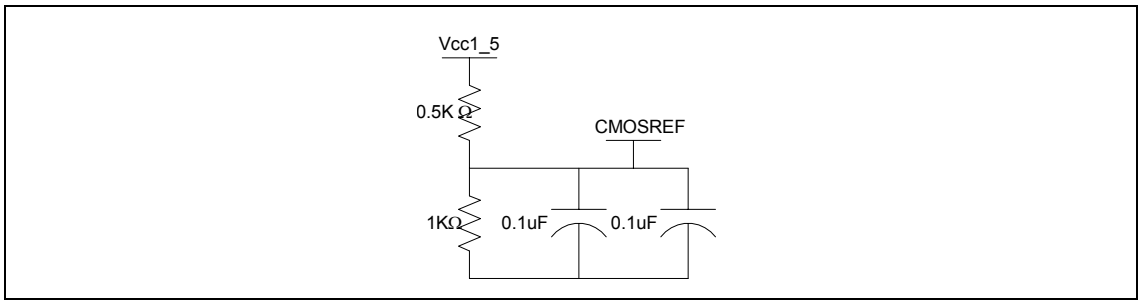


Figure 79. CMOS Reference Voltage



12.2. CK-408 Clock Checklist

12.2.1. Resistor Recommendations

CK-408 Clock – Resistor Recommendations					
Signal	**System Pull-up/ Pull-down**	**Ω**	**Series Damping**	**Notes**	**✓**
3V66[0]			33 Ω		
66BUF[2,0] / 3V66[4,2]			33 Ω	Refer to Intel 830 Chipset Family Design Guide Sec 10.1.3.	
66BUF[1]/ 3V66[3]	See Notes		33 Ω	See GMCH-M signal GBIN. Refer to Intel 830 Chipset Family Design Guide Sec 10.1.3. Use CK408 Pin22(66BUF1) for GBIN. Refer to Figure 79.	
66IN/ 3V66[5]	See Notes		50 Ω	See GMCH-M signal GBOUT. Refer to Intel 830 Chipset Family Design Guide Sec 10.1.2. S3 leakage workaround: Additional 0.01uF series cap within 0.5” of i830 and 240 K pull-down to GND near CK-408. **Required for all i830 SKU silicon.** See Intel 830M Family CRB Sch. p8. Refer to Figure 79.	
CPU[2], CPU[2]#	Pull-down to GND	61.9Ω ±1 %	33 Ω ± 1%	For both: place near CPU. Additional 475Ω ±1% crossover. Refer to Intel 830 Chipset Family Design Guide Sec 10.1.1 Refer to Intel 830M Family CRB Sch. p7 or Figure 78.	
CPU[1], CPU[1]#	Pull-down to GND	61.9Ω ±1 %	33 Ω ± 1%	For both: place near GMCH. Additional 475 Ω ±1% crossover. See Intel 830 Chipset Design Guide Sec 10.1.1. See Intel 830M Family CRB Sch. p7 or Figure 78.	
CPU[0], CPU[0]#	Pull-down to GND	61.9Ω +/- 1%	33 Ω ± 1%	For both: place near ITP. Additional 475 Ω ± 1% Ω crossover. See Intel 830 Chipset Design Guide Sec 10.1.1 See Intel 830M Family CRB Sch. p7 or Figure 78.	
DOT			22 Ω	Can be programmed OFF and damping resistor not needed if using external graphics. Refer to Intel 830 Chipset Design Guide Sec 10.1.7.	
IREF	Pull-down to GND	221Ω ±1%		Pull-down is suitable for Mobile Pentium III Processor-M and Mobile Intel Celeron Processors.	
MULT[0]	Pull-down to GND	10 KΩ		Pull-down is suitable for both Mobile Pentium III Processor-M and Mobile Intel Celeron Processors.	
PCIF[2]			33 Ω	Free running PCI clock. Refer to Intel 830 Chipset Design Guide Sec 10.1.6.	
PCIF[1]	Voltage	27Ω (top)	33 Ω	Voltage divider should be 2-V tolerant for APICCLK	

CK-408 Clock – Resistor Recommendations					
Signal	**System Pull-up/ Pull-down**	**Ω**	**Series Damping**	**Notes**	**✓**
	divider	138 Ω (bottom)		and place near CPU. Refer to Intel 830 Chipset Family Design Guide Sec 10.1.8.1. Intel 830M Family CRB Sch. P7 uses 26.7Ω ±1% and 137 Ω ±1%.	
PCIF[0]	Voltage divider	50 Ω (top) 350 Ω (bottom)	3 3 Ω	Refer to Intel 830 Chipset Design Guide Sec 10.1.8.2. Intel 830M Family CRB Sch. p7 uses 51.1 Ω ±1% and 348 Ω ±1%.	
PCI[6:0]			33 Ω	Refer to Intel 830 Chipset Design Guide Sec 10.1.5, 10.1.6. Intel 830M Family CRB Sch. PCI[1] drives 2 signals with 33 Ω at each trace.	
REF			33 Ω	Intel 830M Family CRB Sch. fans out to drive 3 signals with 33Ω at each trace.	
SCLOCK, SDATA	Pull-up to Vcc3_3	100 KΩ		To SO-DIMM mux. Refer to Intel 830M Family CRB Sch. p12	
S[2]	Pull-up to Vcc3_3	10 KΩ			
S[1:0]				Intel 830M Family CRB Sch. p7 uses 330Ω.	
USB			33 Ω	Refer to Intel 830 Chipset Design Guide Sec 10.1.8	
XTAL_IN, XTAL_OUT				Connect to 14.318-MHz clock. Place crystal within 500 mil of CK-408.	
VSS, VSSA	Tie to GND			8 VSS pins and 1 VSSA pin.	

NOTE: Default tolerance for resistors is ±5% unless otherwise specified.

Figure 80. CK-408 CPUx Signals

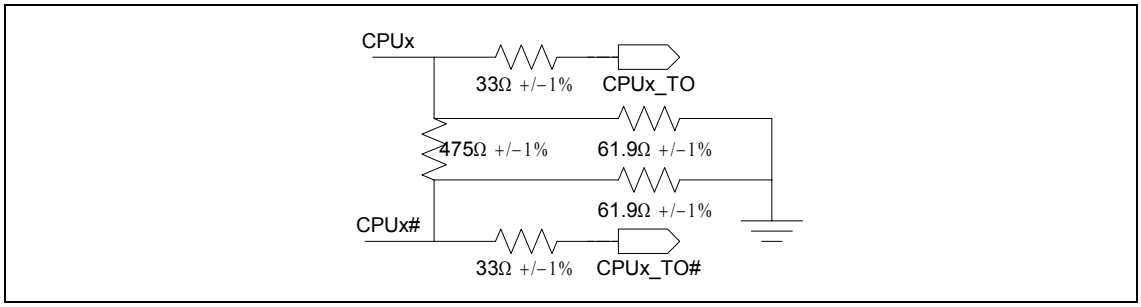
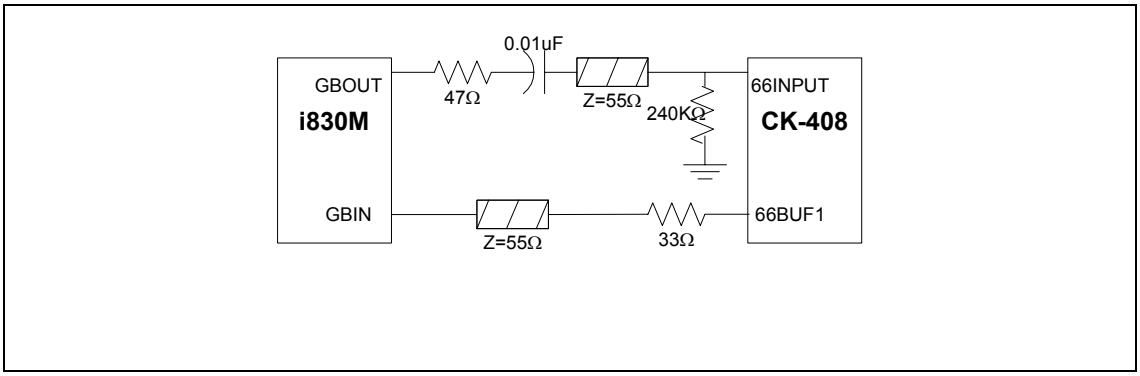


Figure 81. GBOUT Leakage Workaround



12.2.2. Decoupling Recommendations

CK-408 Clock – High Frequency Decoupling Recommendations[1]					
Signal	**Configuration**	**F**	**Qty**	**Notes**	**✓**
VDD	Pull-down to GND	0.01 µF	9	8 VDD pins with Ferrite Bead; Refer to Intel 830M Family CRB Sch.	
VDDA	Pull-down to GND	0.01 µF	1	1 VDDA pin with Ferrite Bead; Refer to Intel 830M Family CRB Sch.	

NOTE: [1]All decoupling guidelines are recommendations based on our reference board design. Customers will need to take their layout & PCB board design into consideration when deciding on their overall decoupling solution.

12.3. GMCH-M Checklist

12.3.1. System Memory Interface

GMCH-M – System Memory Interface					
Signal	**System Pull-up/Pull-down**	**Ω**	**Series Damping**	**Notes**	**✓**
SM_CAS#, SM_RAS#, SM_WE#			10 Ω	Refer to Intel 830 Chipset Design Guide Sec 4.1.1	
SM_CLK[3:0]			10 Ω	Refer to Intel 830 Chipset Design Guide Sec 4.1.4	
SM_BA[1:0], SM_MA[12:0]			10 Ω	Refer to Intel 830 Chipset Design Guide Sec 4.1.1	
SM_OCLK				0.15" ± 50mil pin-to-pin trace length to SM_RCLK. Refer to Intel 830 Chipset Design Guide Sec 4.1.5	
SM_RCLK	Use C placeholder near SM_RCLK			0.15" ± 50mil pin-to-pin trace length to SM_OCLK. Refer to Intel 830 Chipset Design Guide Sec 4.1.5 Capacitor is "No stuff" in the latest Intel 830M Family CRB schematic	

12.3.2. Miscellaneous Signals

GMCH-M – Miscellaneous Signals					
Signal	**System Pull-up/ Pull-down**	**Ω**	**F**	**Notes**	**✓**
Host Interface Signals					
ADS#, BNR#, BPRI#, CPURST#, DBSY#, DEFER#, DRDY#, HA[31:3]#, HD[63:0]#, HIT#, HITM#, HLOCK#, HREQ[4:0]#, HTRDY#, RS[2:0]#				Route all signals between CPU and GMCH-M with board trace impedance. Refer to Intel 830 Chipset Design Guide Sec 3.3 H_CPURST# also drives H_RESETX# (for ITP connector) in Intel 830M Family CRB.	
General Purpose I/O Signals					
DDC1CLK, DDC1DATA	Pull-up to Vcc3_3	2.2 K-10 KΩ	10 pF	1. For 830M and 830MP AGP designs 10K-100K pullups are acceptable values as these signals are not used in AGP design. 2. For 83-M/MGUMA design's Non-5-V tolerant, Q-Switch required for 5-V device support. Place caps near VGA connector. Refer Intel 830 Chipset Design Guide Sec 6.5. Used for CRT DDC support.	

GMCH-M – Miscellaneous Signals					
Signal	**System Pull-up/ Pull-down**	**Ω**	**F**	**Notes**	**✓**
DDC2CLK, DDC2DATA	Pull-up to Vcc3_3	2.2 K-10 KΩ		1. For 830M and 830MP AGP designs 10K-100K pullups are acceptable values as these signals are not used in AGP design. 2. For 830M and 830MG UMA design, (non-5-V tolerant), Q-Switch required for 5-V device support. Refer to Intel 830 Chipset Design Guide Sec 6.5. Used for panel EDID support, not required if panel does not support.	
I2CCLK, I2CDATA	Pull-up to Vcc3_3	2.2 K-10 KΩ		1. For 830M and 830MP AGP designs 10K-100K pullups are acceptable values as these signals are not used in AGP design. 2. For 830M and 830MG UMA design, non 5-V tolerant, Q-Switch required for 5-V devicesupport. Refer to Intel 830 Chipset Design Guide Sec 6.5 for further details. Used for DVOA GMBUS	
Clock Signals					
GBIN, GBOUT	See Sec 5.1 for topology info			See Sec 12.3.1 and Figure 79 for topology info and S3 leakage workaround.	
DREFCLK	See Notes	4.7 K-10 KΩ		1. For Intel 830M and 830MP external graphics only: Pull down this signal to ground. Not requiredto route out to CK408. 2. For UMA designs route out to CK408. Pullup not required.	
Hub Interface Signals					
HL[10:0]				Route all signals between CPU and GMCH-M based on board trace impedance. Refer to Intel 830 Chipset Design Guide Sec 8.1	
Ground Signals					
VSS[36:0], VSS_LM_[37:0], VSSP_SM[19:0], VSSP_AGP[8:0], VSS_H[16:0], VSSPCMOS_LM[2:0], VSSP_HUB[1:0], VSSP_IO[2:0], VSSP_DVO[2:0], VSSA_DAC, VSSA_CPLL, VSSA_HPLL	Tie to GND				
VSSA_DPLL[1:0]				**For internal graphics:** If possible route to negative term. of capacitor in the RLC circuit. Intel 830M Family CRB Sch. **For external graphics:** Tie the signals to ground	

12.3.3. Resistive Compensation

GMCH-M – Resistive Compensation				
Signal	**System Pull-up/Pull-down**	**Ω**	**Notes**	**✓**
AGP_RCOMP/ DVOBC_RCOMP	Pull-down to GND	54.9 Ω ±1%	Used to control I/O buffer impedance to AGP or DVO B/C devices. Pull-down required for all 830 SKU's. Equal to board impedance. Refer to Intel 830 Chipset Design Guide Sec 5.6.3	
DVOA_RCOMP	Pull-down to GND	54.9 Ω ±1%	Used to control I/O buffer impedance to DVOA devices. Pull-down required for all SKU's. Equal to board impedance.	
GTL_RCOMP	Pull-down to GND	80.6 Ω ±1%		
HUB_RCOMP	Pull-down to GND	54.9 Ω ±1%	Equal to board impedance. Refer to Intel 830 Chipset Design Guide Sec 8.1	
SM_RCOMP	Pull-down to GND	27.5 Ω ±1%	Resistance value is half of board impedance. Refer to Intel 830 Chipset Design Guide Sec 4.6.	

12.3.4. Decoupling Recommendations

GMCH-M – High Frequency Decoupling Recommendations[1]					
Signal	**Configuration**	**F**	**Qty**	**Notes**	**✓**
GTL_REF[B:A]	Pull-down to GND	0.1 µF	2		
HLREF	Pull-down to GND	0.1 µF 0.01 µF	1 1	Place close to GMCH-M.	
SM_REF[B:A]	Pull-down to GND	0.1 µF	1	Place close to GMCH-M.	
Vcc1_25 (PSB)	Pull-down to GND	0.1 µF 10 µF	10 1	Distribute as close as possible to GMCH-M Processor Quadrant. Intel 830M Family CRB Sch. uses 20 x 0.1 µF caps. See p10	
Vcc1_25 (Core)	Pull-down to GND	0.1 µF 10 µF	10 1	Intel 830M Family CRB Sch. uses 28 x 0.1 µF caps. See p10	
Vcc1_5	Pull-down to GND	0.1 µF 82 pF	9 4	Distribute as close as possible to GMCH-M AGP/DVO Quadrant. Refer to Intel 830M Family CRB Sch. p10	
Vcc1_8	Pull-down to GND (Pull-down to GND)*	0.1 µF 0.01 µF 82 pF	4 &(2)* (2)* 2	Distribute as close as possible to GMCH-M Local Memory Quadrant. *Additional pull-down network to GND of four capacitors shall be distributed as close as possible to VCCPCMOS_LM. Refer to Intel 830M Family CRB Sch.	
VccSus3_3	Pull-down to GND	0.1 µF	12 &(2)*	Distribute as close as possible to GMCH-M System Memory Quadrant.	

GMCH-M – High Frequency Decoupling Recommendations[1]					
Signal	**Configuration**	**F**	**Qty**	**Notes**	**✓**
	(Pull-down to GND)*	82 pF	4	*Additional pull-down network to GND of two 0.1-µF capacitors shall be distributed as close as possible to IO Quadrant. Refer to Intel 830M Family CRB Sch.	
VCC, VDD_LM	Pull-down to GND	68 pF	1	Close to VDD_LM, near pins AE15 and AE16 on U6E. For external graphics, decoupling is still required for VDD_LM. Refer to Intel 830M Family CRB Sch.	
VCC_LM	Pull-down to GND	68 pF	1	For external graphics, decoupling is still required.	
VCCA_CPLL, VCCA_HPLL	Pull-down to GND	0.1 µF	1	Close to VDD_LM, near pins AE15 and AE16 on U6E. Refer to Intel 830M Family CRB Sch.	

12.3.5. Reference Voltage Dividers

GMCH-M – Reference Voltage Dividers[1]				
Signal	**System Pull-up/Pull-down**	**Ω**	**Notes**	**✓**
HLREF	Voltage divider with decoupling caps.	301 Ω ±1% (both)	See Sec 12.4.4 for decoupling. Place divider pair in middle of bus. Place capacitor near GMCH-M. R value range is 100 Ω – 1 KΩ. Divided voltage is [1/2]*1.8 V = 0.9 V. Refer to Intel 830 Chipset Design Guide Section 9.4 Refer to Intel 830M Family CRB Sch. uses 301 Ω ±1% or Figure 81	
SM_REF[B:A]	Voltage divider with decouling caps.	249 Ω ±1% (top) 49.9 Ω ±1% (bottom)	See Sec 6.4 for decoupling. Place capacitor near GMCH-M. R value range is 100 Ω – 1 KΩ. Divided voltage is [1/6]*3.3 V = 0.55 V. Refer to Intel 830 Chipset Family Datasheet Sec 3.4. See Intel 830M Family CRB Sch or Figure 80.	

NOTE: [1]All decoupling guidelines are recommendations based on our reference board design. Customers will need to take their layout, & PCB board design into consideration when deciding on their overall decoupling solution.

Figure 82. System Memory Reference Voltage

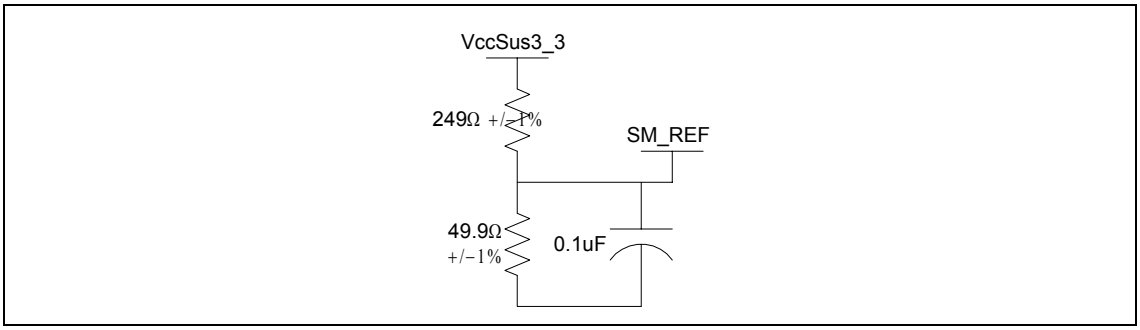
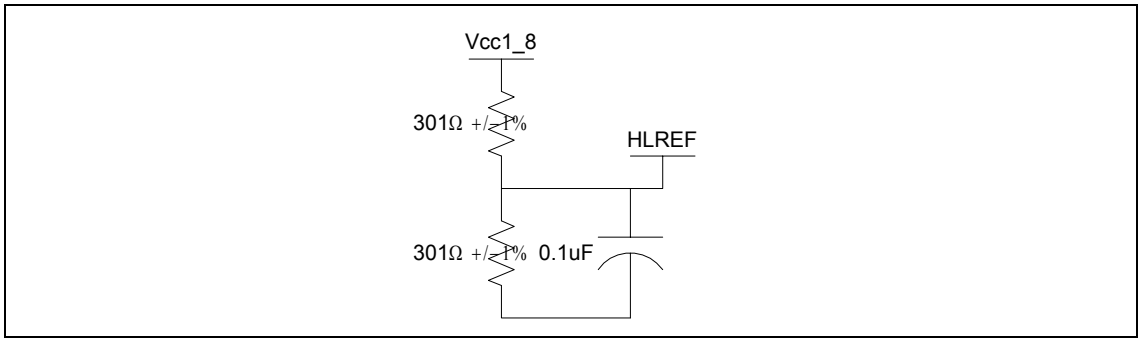


Figure 83. Hub Interface Reference Voltage



12.3.6. Intel 830MP and 830M Discrete AGP Device Interface

12.3.6.1. Resistor Recommendations

Intel 830MP/830M Chipset GMCH-M AGP Interface – Resistor Recommendations					
Signal	**System Pull-up/Pull-down**	**Ω**	**Series Damping**	**Notes[2]**	**✓**
AD_STB[0]/ DVOB_CLK, **AD_STB[0]#**/ DVOB_CLK#	See Notes			For AD_STB[0] and AD_STB[0]# pull-up recommendations, see “SB_STB, ST[2:0]” and “SB_STB#”, respectively.	
AD_STB[1]/ DVOC_CLK, **AD_STB[1]#**/ DVOC_CLK#	See Notes			For AD_STB[1] and AD_STB[1]# pull-up recommendations, see “SB_STB, ST[2:0]” and “SB_STB#”, respectively.	
G_DEVSEL# / M_I2C_DATA, **G_FRAME#** / M_DDC1_DATA, **G_IRDY#** / M_I2C_CLK , **G_TRDY#** / M_DDC1_CLK **G_GNT#, G_REQ#, G_STOP#, PIPE#, RBF#, WBF#**	See Notes			No pull-up required. AGP signals have internal pull up. Refer to Intel 830 Chipset Design Guide Sec 5.3.6. Refer to Intel 830M Family CRB Sch.	
G_PAR/ DVOBC_Detect	See Notes			No pull-up resistor required. Internal pull-up to support AGP is by default 0 = DVO B/C Device 1 = AGP Device For proper DVO B/C device detection, 330Ω pull-down to GND is recommended. Refer to Intel 830 Chipset Design Guide Sec 5.3.6. Refer to Intel 830M Family CRB Sch.	
SB_STB, ST[2:0]	See Notes			No pull-up required. Refer to Intel 830 Chipset Design Guide Sec 5.3.6.	
SB_STB#	See Notes			No pull-down required. Refer to Intel 830 Chipset Design Guide	

Intel 830MP/830M Chipset GMCH-M AGP Interface – Resistor Recommendations					
Signal	System Pull-up/Pull-down	Ω	Series Damping	Notes[2]	✓
				Sec 5.3.6.	

NOTE: Default tolerance for resistors is ± 5% unless otherwise specified.

12.3.6.2. PERR#, SERR# Resistor Recommendations

GMCH-M PERR#, SERR# – Resistor Recommendations					
Signal	System Pull-up/ Pull-down	Ω	Series Damping	Notes	✓
SERR#, PERR#	See Notes			PERR# and SERR# are not supported in the Intel 830 AGP interface. Refer to Intel 830 Chipset Family Datasheet sec 3.2.5. For AGP controllers that support PERR# and SERR#, tie signals directly to Vcc1_5 using 8.2 KΩ pull-ups.	

12.3.6.3. AGP/DVOB & DVOC Decoupling Recommendations

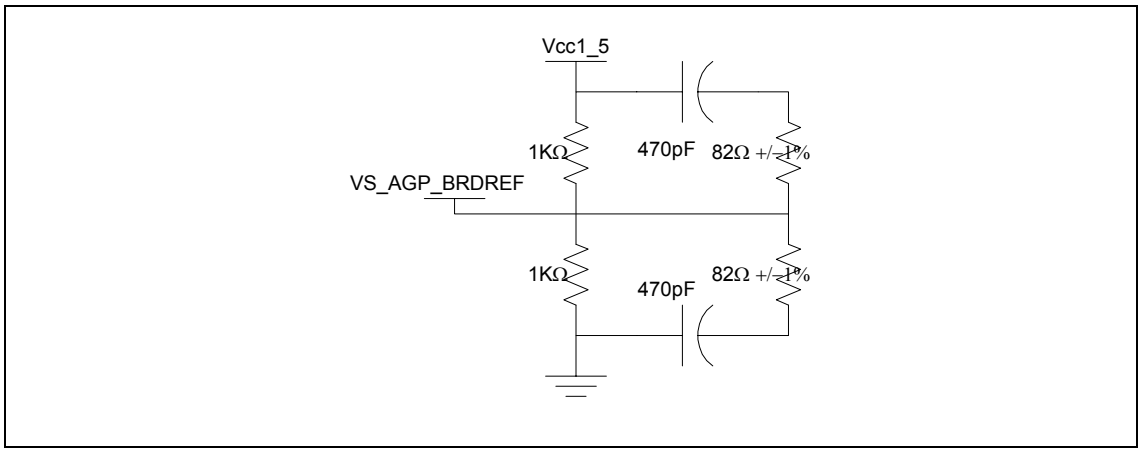
GMCH-M AGP – High Frequency Decoupling Recommendations[1]					
Signal	Configuration	F	Qty	Notes	✓
Vcc1_5	Pull-down to GND	0.01 µF 82 pF	7 3	Refer to Intel 830M Family CRB Sch. p16, signal VDDQAGP_CONN.	
AGPREF	Pull-down to GND	0.1 µF	1	[1/2]*VDDQ reference voltage input for the AGP interface generated by video controller. See Sec 12.4.6.4 for more details. Refer to Intel 830M Family CRB Sch. p16, signal VS_AGP_CRDREF.	
Vcc3_3	Pull-down to GND	0.01 µF	7	See Intel 830M Family CRB Sch. p16	
Vcc5	Pull-down to GND	0.01 µF	3	See Intel 830M Family CRB Sch. p16	
Vcc12	Pull-down to GND	0.01 µF	1	See Intel 830M Family CRB Sch. p16	

12.3.6.4. AGP Vref Reference Voltage Dividers

GMCH-M AGP Interface – Reference Voltage Dividers[1]				
Signal	System Pull-up/ Pull-down	Ω	Notes	✓
VS_AGP_BRDREF	See Figure 82	1 KΩ (both in divider) 82 Ω ±1% (both R in series with C)	Place near the Intel 830MP/830M Chipset GMCH-M; Required reference voltage. [1/2]*VDDQ to video card. Generation of AGPREF voltage is platform dependent. VS_AGP_BRDREF can be used for the AGPREF input in designs where the video controller is down on motherboard or does not generate the voltage on a daughtercard. Required as DVOVREF for DVO devices. Refer to Intel 830M Family CRB Sch. p16 or Figure 82	

NOTE: [1]All decoupling guidelines are recommendations based on our reference board design. Customers will need to take their layout, & PCB board design into consideration when deciding on their overall decoupling solution.

Figure 84. AGP Board Reference Voltage



12.3.7. Intel 830M and 830MG Internal Graphics Interface

12.3.7.1. CRT / DVO A Interface

GMCH-M CRT / DVO A Interface – Resistor Recommendations						
Signal	**System Pull-up/Pull-down**	**Ω**	**F**	**Series Damping**	**Notes**	**✓**
DVOA Resistor Recommendations						
DVOA_CLK, DVOA_CLK#					Routing clarification to VCH: • DVOA_CLK (Intel 830M/ 830MG Chipset GMCH-M ball AJ24) is the primary clock that routes to DVOCLKIN[0] (VCH ball M8) • DVOA_CLK# (Intel 830M / MG Chipset GMCH-M ball AG24) is the primary clock that routes to DVOCLKIN[1] (VCH ball N8)	
DVOA_CLKINT	Pull-up to Vcc1_5	4.7 K– 100 KΩ			Pull-up required if DVOA not implemented. Refer to Intel 830 Chipest Family Design Guide Sec 6.5.1. DVOA_CLKIN used for TV encoder DVOA_INT# for VCH	
DVOA_FLD/ STL	Pull-down to GND	4.7 K – 100 KΩ			Pull-down required if DVOA not implemented. Refer to Intel 830 Chipset Family Design Guide Sec 6.5.1. DVOA_FLD used for TV encoder DVOA_STALL used for VCH	
DVOA_INTR#	Pull-up to Vcc1_5	4.7 K – 100 KΩ			Pull-up required if DVOA not implemented. Refer to Intel 830 Chipset Family Design Guide Sec 6.5.1.	
CRT Resistor Recommendations						
RED, GREEN, BLUE	LC Pi filter – two 3.3pF and one ferrite bead	75 Ω	3.3 pF		Filter for high freq noise and EMI reduction. Place near CRT. For external graphics, leave unconnected (NC). Refer to Intel 830 Chipset Family Design	

GMCH-M CRT / DVO A Interface – Resistor Recommendations						
Signal	System Pull-up/Pull-down	Ω	F	Series Damping	Notes	✓
	(75Ω @ 100MHz)				Guide Sec 6.1.1. Intel 830M Family CRB Sch. uses 75 Ω ±1%. See p15.	
RED#, GREEN#, BLUE#	Pull-down to GND	37.5 Ω	0.1 µF		For external graphics, leave unconnected (NC). Refer to Intel 830 Chipset Family Design Guide Sec 6.1.1. Intel 830M Family CRB Sch. uses 37.4Ω ±1%. See p9	
REFSET	Pull-down to GND	255 Ω ±1%			For external graphics, leave unconnected (NC). Refer to Intel 830 Chipset Family Design Guide Sec 6.1.2.	
VSYNC, HSYNC			10 pF	40 Ω	Place caps near VGA connector. Refer to Intel 830 Chipset Family Design Guide Sec 6.1.9. For AGP graphics, leave unconnected (NC). Intel 830M Family CRB Sch. uses 39Ω. See p15.	

NOTE: Default tolerance for resistors is ±5% unless otherwise specified.

12.3.7.2. VCCA_DPLL[1:0] RLC Circuit

GMCH-M – VCCA_DPLL[1:0] RLC Circuit			
Device	Value	Notes	✓
R	1Ω	Refer to Intel 830 Chipset Family Design Guide Sec 7.1	
L	0.1 uH	Refer to Intel 830 Chipset Family Design Guide Sec 7.1	
C	0.1 µF, 100 µF_16 V (in parallel)	Refer to Intel 830 Chipset Family Design Guide Sec Sec 7.1 For internals graphics, recommendation is to connect VSSA_DPLL[1:0] to the negative terminals of the caps. For external garphics, RLC is not required, and VSSA_DPLL[0:1] should be connected to digital ground.	

12.3.7.3. CRT Decoupling Recommendations

GMCH-M CRT / DVO A Interface – High Frequency Decoupling Recommendations[1]					
Signal	Configuration	F	Qty	Notes	✓
Vcc1_5	Pull-down to GND	0.1 µF 10 µF_10 V	3 1		
Vcc1_8	Pull-down to GND	0.1 µF	1	Refer to Intel 830M Family CRB Sch. p15	
Vcc3_3	Pull-down to GND	0.1 µF 10 µF_10 V	3 1		
Vcc5	Pull-down to GND	0.1 µF	2		

12.3.7.4. DVOA Connector Reference Voltage Dividers

GMCH-M DVO A – Reference Voltage Dividers[1]				
Signal	**System Pull-up/Pull-down**	**Ω**	**Notes**	**✓**
0.7 V DVO VREF			Actual implementation will depend on DVOA device used. Refer to Intel 830M Family CRB Sch. p14, signal V0-7S_DVO_VREF.	
2.5 V DVO VREF			Not required to support Intel VCH part. Refer to Intel 830M Family CRB Sch. p14, signal V2-5S_DVO _VREF.	

NOTE: [1]All decoupling guidelines are recommendations based on our reference board design. Designers will need to take their layout, & PCB board design into consideration when deciding on their overall decoupling solution.

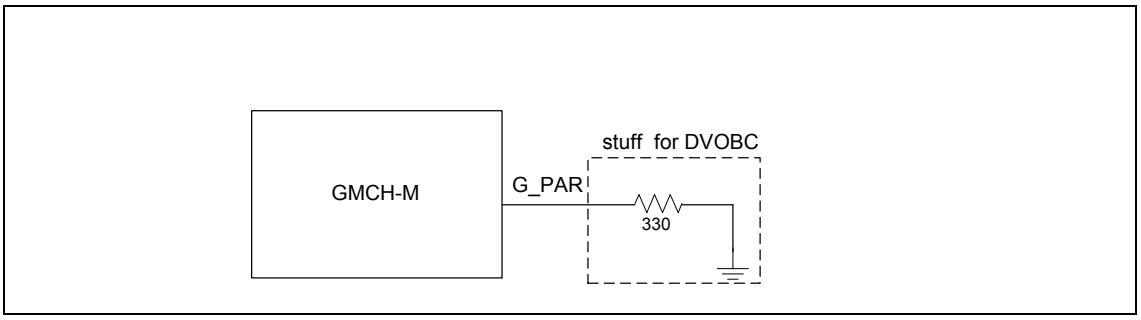
12.3.7.5. DVOBC Interface

DVO B/C Interface – Resistor Recommendations					
Signal	**System Pull-up/ Pull-down**	**Ω**	**Series Damp-ing**	**Notes**	**✓**
AGPBUSY#				When 830M UMA graphics is used, this ICH3-M signal must be connected to the AGP_BUSY# output of the GMCH-M. Refer to Checklist Section 12.6.3 for AGP_BUSY# Design Requirement. Refer to Intel 830 Chipset Family Design Guide Sec 5.6.4 and Sec. 11.9.8 for further details.	
AD_STB[0]/ **DVOB_CLK**, AD_STB[0]#/ **DVOB_CLK#**	See notes			Routing clarification to DVO interface: • DVOB_CLK (GMCH-M ball L29) is the primary clock that connects to DVOCLKIN[0] • DVOB_CLK# (GMCH-M ball L28) is the secondary clock that connects to DVOCLKIN[1]	
AD_STB[1]/ **DVOC_CLK**, AD_STB[1]#/ **DVOC_CLK#**	See notes			Routing clarification to DVO interface: • DVOC_CLK (GMCH-M ball U29) is the primary clock that connects to DVOCLKIN[0] • DVOC_CLK# (GMCH-M ball U28) is the secondary clock that connects to DVOCLKIN[1]	
M_I2C_CLK / G_IRDY#, **M_I2C_DATA** / G_DEVSEL#, **M_DDC1_CLK** / G_TRDY#, **M_DDC1_DATA**/ G_FRAME#, **DVOBC_CLKINT#** / G_AD13,	See notes			If these signals are not used, then need to **pull-up** to Vcc 1_5 through a 4.7K to 100K ohms resistor. Refer to Intel 830 Chipset Design Guide Sec 6.5	
DVOB_FLD/STL/G_AD14, **DVOC_FLD/STL**/G_AD31	See notes			if these signals are not being used, a **pull down** through a 4.7K to 100 KΩ resistor is required. Refer to Intel 830 Chipset Design Guide Sec 6.5	
G_PAR/ **DVOBC_ DETECT**	See notes			For proper DVO B/C device detection, 330Ω pull-down to GND is recommended. 0 = DVO B/C Device 1 = AGP Device	

DVO B/C Interface – Resistor Recommendations					
Signal	System Pull-up/ Pull-down	Ω	Series Damp-ing	Notes	✓
				Refer to Intel 830 Chipset Design Guide Sec 6.3.6 Refer to Intel CRB Sch. p16 or Figure 83	

NOTE: Default tolerance for resistors is ±5% unless otherwise specified.

Figure 85. DVO B/C Interface Strap

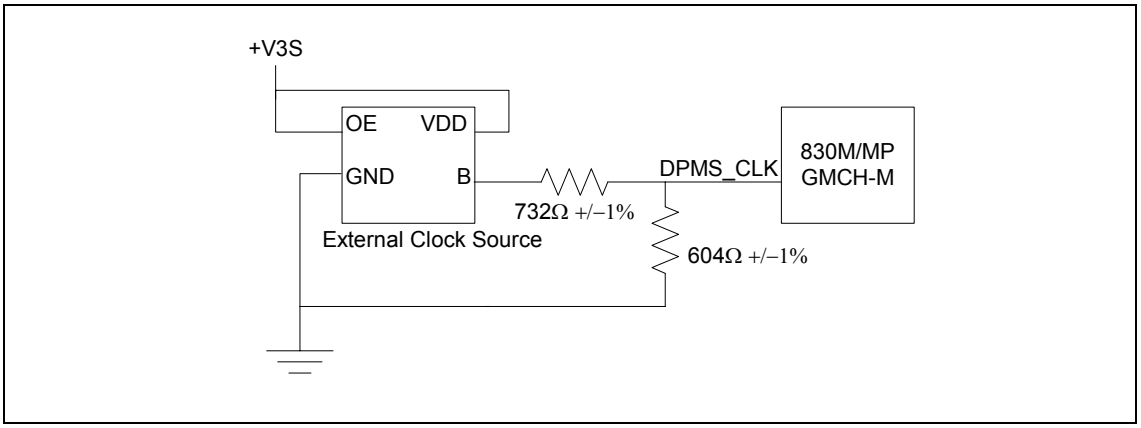


NOTE: Strapping Option for AGP or DVO B/C interface. [AGP= default; 0 = DVOB/C].

12.3.7.6. DPMS Interface

GMCH-M DPMS Interface				
Signal	System Pull-up/Pull-down	Ω	Notes	✓
DPMS_CLK			This signal is muxed with G_AD30. When intergrated graphics is used, this signal is needed to provide the necessary clock source for D1/S1 state support. This signal is 1.5 -V tolerance only. Refer to Intel 830 Chipset Design Guide Sec 11.9.7. Refer to Figure 84 and Intel CRB pg 9 for reference.	

Figure 86. DPMS Supports



12.3.8. Intel 830 Chipset Family DVO A Strapping Options

Intel 830 Chipset family GMCH-M – DVO A Strapping Options

Signal	System Pull-up/Pull-down	Ω	Notes	✓
DVOA_D0			0 = Reserved 1 = 133 MHz (default)	
DVOA_D1	See Notes		0 = IOQD 1 1 = IOQD 8 (default) No pull-up required, otherwise 2.2 KΩ pull-down to GND for IOQD 1 support.	
DVOA_D5	Pull-up to Vcc1_5	2.2 KΩ	0 = Desktop (default) 1 = Mobile Required pull-up for SW Mobile detection.	
DVOA_D6	See Notes		0 = Dual ended termination (default) 1 = Single ended termination No pull-down required, otherwise 2.2 KΩ pull-up to Vcc1_5 for single ended termination option.	
DVOA_D7	See Notes		0 = Normal operation (default) 1 = XOR Chain test mode No pull-up required, otherwise 2.2 KΩ pull-up to Vcc1_5 for XOR Chain test mode initialization. Refer to Intel 830 Chipset Family Datahseet Sec 3.5 for details.	
DVOA_D8	See Notes		0 = Normal operation (default) 1 = Tri-state all Intel 830 Chipset family GMCH-M outputs No pull-up required, otherwise 2.2 KΩ pull-up to Vcc1_5 for tri-stated ouput mode. Refer to Intel 830 Chipset Family Datahseet Sec 3.5 for details	

12.3.9. Intel 830 Chipset Family Reserved Signals

12.3.9.1. Graphics Memory (Reserved signals) Resistor Recommendations

GMCH-M Graphics Memory Interface – Resistor Recommendations					
Signal	System Pull-up/Pull-down	Ω	Series Damping	Notes[2]	✓
CMD	See Notes			Leave as NC (“Not Connected”)	
CFM, CFM#	See Notes			Leave as NC (“Not Connected”)	
CTM, CTM#	Pull-down to GND	10 KΩ			
DQ_A[7:0], DQ_B[7:0]	See Notes			Leave as NC (“Not Connected”)	
RAM_REF[B:A]	Voltage Divider	576 Ω ±1% (top) 2 kΩ ±1% (bottom)		Resistor divider pair required for internal and external graphics solutions. For external graphics solution, 1% tolerance not needed.	
RQ[7:0]	See Notes			Leave as NC (“Not Connected”)	
SCK	See Notes			Leave as NC (“Not Connected”)	
SIO	See Notes			Leave as NC (“Not Connected”)	
VccSus1_8	Pull-down to GND	0.1 µF	2		

GMCH-M Graphics Memory Interface – Resistor Recommendations					
Signal	**System Pull-up/Pull-down**	**Ω**	**Series Damping**	**Notes[2]**	**✓**
Vcc1_8	Pull-down to GND	0.1 µF 68 pF	8 8		

12.4. VCH Checklist

This VCH checklist reflects the Intel® 830M Chipset VCH Winnie customer reference daughter card schematics.

12.4.1. VCH Resistor Recommendations

VCH – Resistor Recommendations					
Signal	**System Pull-up/ Pull-down**	**Ω**	**Series Damping**	**Notes**	**✓**
DVO Interface					
DVOSTALL/ DVOCLKOUT	Pull-down to GND	75 Ω ±1%	15 Ω ±1%	VCH signal is 1.8 V, GMCH interface is 1.5 V. GMCH-M is Non-1.8-V tolerant. Refer to Intel VCH Reference Daughtercard Sch. p3 DVOSTALL for panel operation DVOCLKOUT for TV encoder support	
DVOr Interface					
DVOrCLKIN	Pull-down to GND	10 KΩ		Refer to Intel VCH reference daughtercard Sch. p2	
DVOrCOMP	Pull-up to Vcc1_8	36.5Ω ±1%		Equal to [2/3]*board impedance.Refer to Intel VCH reference daughtercard Sch. uses 40.2 Ω ±1%. See p3.	
CMOS LCD Interface					
DE, FLM, LP			39 Ω	If not using VCH, leave unconnected (NC). Zeros will be driven when panel is disabled. Refer to Intel VCH reference daughtercard Sch. p2.	
P[35:0]			39 Ω	If not using VCH, leave unconnected (NC). Zeros will be driven when panel is disabled. Refer to Intel VCH reference daughtercard Sch. p2.	
SHFCLK			39 Ω	If not using VCH, leave unconnected (NC). Output tristated when panel is disabled. Refer to Intel VCH reference daughtercard Sch. p2.	
GM BUS Interface					
GMBSDA	Pull-up to Vcc3_3	2.2 K-10 KΩ		When VCH is implemented, GMBSDA needs to pull up	
GMBSCL	Pull-up to Vcc3_3	2.2 K-10 KΩ		When VCH is implemented, GMBSCL needs to pull up	
LVDS LCD Interface					
VREF_HI	Pull-up to Vcc1_8	150 Ω		Test pin. See Intel VCH reference daughtercard Sch. p2	
VREF_LO	Pull-down to GND	150 Ω		Test pin. See Intel VCH reference daughtercard Sch. p2	
Miscellaneous					
ENAVDD			100 KΩ	Input signal to base of BJT. See Intel VCH reference daughtercard Sch. p5 (The series damping resistor is there to prevent overshooting)	
TESTIN	Pull-down to GND			Tie directly to GND. Refer to Intel VCH reference daughtercard Sch. p3	

NOTE: Default tolerance for resistors is ±5% unless otherwise specified.

12.4.2. VCH Decoupling Recommendations

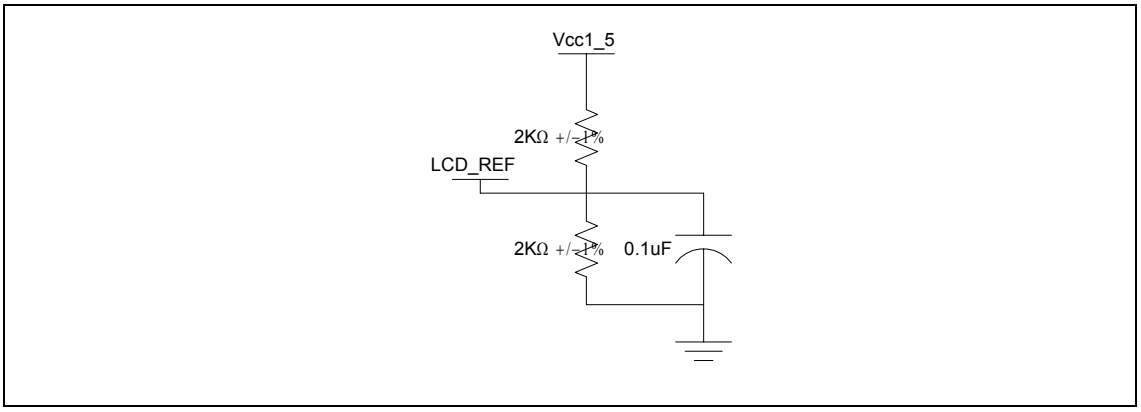
VCH – Decoupling Recommendations[1]					
Signal	**Capacitor Value**	**Qty**	**Placement**	**Notes**	✓
Vcc0_7	0.1 µF 10 µF	1 1	Pull-down to GND		
Vcc1_8	0.1 µF 10 µF	7 1	Pull-down to GND		
VCCA, VCCBA, VCCDA	0.1 µF	1	Pull-down to GND	All 3 signals can share one cap and and pull-up to Vcc1_8 through one ferrite bead.	

12.4.3. VCH Voltage Dividers

VCH – Voltage Dividers[1]				
Signal	**Pull-up/Pull-down**	**Ω**	**Notes**	✓
LCD_VREF	Voltage divider with 0.1 µF across bottom resistor	2 KΩ ±1%	Pin is connected to VREF3 (0.7 V) input of DVO connector. Refer to Intel 830M Family CRB Sch. p14 or Figure 85 Refer to Intel VCH refernce daughtercard Sch. p4	
VREF_5	Voltage divider with 0.1 µF across bottom resistor	2 KΩ ±1%	Intel VCH does not require 2.5-V reference voltage. See Intel 830M Family CRB Sch. p14. Refer to Intel VCH refernce daughtercard Sch. p4	

NOTE: [1]All decoupling guidelines are recommendations based on our reference board design. Customers will need to take their layout, & PCB board design into consideration when deciding on their overall decoupling solution.

Figure 87. LCD Reference Voltage



12.4.4. VCH Strapping Options

VCH – Strapping Options				
Signal	**Strap Description**	**Ω**	**Notes**	**✓**
GPIO[1:0]	Default state is NC.		Used for external TV encoder or DVI transmitter power down control.	
GPIO[5:2]	Can be used for panel ID.	10-4.7 KΩ	Can be used for Panel Select Detect. Default state is GPI with Internal weak pull down.	
GPIO6	For normal VCH operation pin has to be read as low. Note: default setting is for internal pull down.	10-4.7 KΩ	Default state is GPI with Internal weak pull down.	
GPIO[8:7]	Used for GMBus base address.	10-4.7 KΩ	Used for GMBus address select. Default state is GPI with Internal weak pull down.	

12.5. ICH3-M Checklist

Note: All inputs to the ICH3-M must not be left floating. Many GPIO signals are fixed inputs that must be pulled up to different sources.

12.5.1. ICH3-M Resistor Recommendations

ICH3-M – Resistor Recommendations					
Signal	**System Pull-up/ Pull-down**	**Ω**	**Series Damping**	**Notes**	**✓**
PCI Resistor Recommendations					
CLKRUN#	Pull-up to Vcc3_3	10 KΩ		Refer to Intel 830M Family CRB Sch. p21	
FRAME#, IRDY#, TRDY#, STOP#	Pull-up to Vcc3_3	8.2 KΩ		Alternative system can be 2.7 KΩ pull-up to Vcc5.	
PERR#, SERR#, DEVSEL#, PLOCK#	Pull-up to Vcc3_3	8.2 KΩ		Alternative system can be 2.7 KΩ pull-up to Vcc5.	
GPIO[0]/REQ[A]# GPIO[1]/REQ[B]#/ REQ[5]#, REQ[4:0]#	Pull-up to Vcc3_3	8.2 KΩ		Alternative system can be 2.7 KΩ pull-up to Vcc5.	
PCIRST#			22 Ω-47 Ω	Should be buffered to form IDE_RST# for improved signal integrity. Refer to Intel 830 Chipset Family Design Guide Sec 10.1.2	
PME#				Has integrated pull-up of 18 K – 42 KΩ	
GNT[4:0]#				External pull-up not required because they are actively driven by the ICH3-M. If external resistors implemented, they must be pulled up to Vcc3_3.	
GPIO[16]/ GNT[A]#, GPIO[17]/ GNT[B]#/GNT[5]#				Has integrated pull-up of 24 KΩ. GNT[A] has an added strap function of “top block swap”. The signal is sampled on the rising edge of PWROK. Default value is high or disabled due to pull-up. A Jumper to a pull down resistor can be added to manually enable the function.	
GPIO Resistor Recommendations					
GPIO[7]	Pull-up to Vcc3_3	10 KΩ		Fixed as input only. See Intel 830M Family CRB Sch. p21.	
GPIO[25,27,28]	See Notes			Resume well GPIO. Output “HIGH” as default. Signal can be left open (NC) if unused or if BIOS does not configure it as an input. Also see ICH3-M Datasheet for more information.	
Interrupt Interface Resistor Recommendations					
IRQ[15:14]	Pull-up to Vcc3_3	8.2 KΩ		Open drain outputs from IDE drive.	
PIRQ[D:A]#	Pull-up to Vcc3_3	8.2 KΩ		Alternative system can be 2.7 KΩ pull-up to Vcc5.	
PIRQ[E]#/ GPIO[2]	Pull-up to Vcc3_3 or Pull-down to GND.	10 KΩ		Bluetooth Strapping option 0 = Disable	

ICH3-M – Resistor Recommendations					
Signal	**System Pull-up/ Pull-down**	**Ω**	**Series Damping**	**Notes**	**✓**
	See Notes			1 = Enable (default) Refer to Intel 830M Family CRB Sch. p18	
PIRQ[H:F]#/ GPIO[5:3]	Pull-up to Vcc3_3	8.2 KΩ		Alternative system can be 2.7 KΩ pull-up to Vcc5.	
SERIRQ	Pull-up to Vcc3_3	8.2 KΩ			
APICCLK	See Sec 5.1, PCIF0 for topology info			**If the APIC is not used:** Recommended Implementation: Disable IOAPIC in BIOS by setting (D31: F0) Offset: D0-D3h, bit 8 (0 = disable) and using the configuration in Figure 86. Refer to Intel 830M Family CRB Sch. Minimum Implementation: Disable IOAPIC in BIOS by setting (D31: F0) Offset: D0-D3h, bit 8 (0 = disable) and using the configuration in Figure 87. See "PICCLK" in Sec 12.2.1 for CPU recommendations.	
APICD[1:0]	See Fig 8-1 and Fig 8-2			**If the APIC is not used:** See recommendations for "APICCLK". See Intel 830M Family CRB Sch. p7	
CPU Interface Resistor Recommendations					
CPUPWRGD	See Sec 12.3.1			See "PWRGOOD" in Sec 12.2.1 for pull-up recommendations.	

NOTE: Default tolerance for resistors ± 5% unless otherwise specified.

Figure 88. Recommended IOAPIC Disable Topology

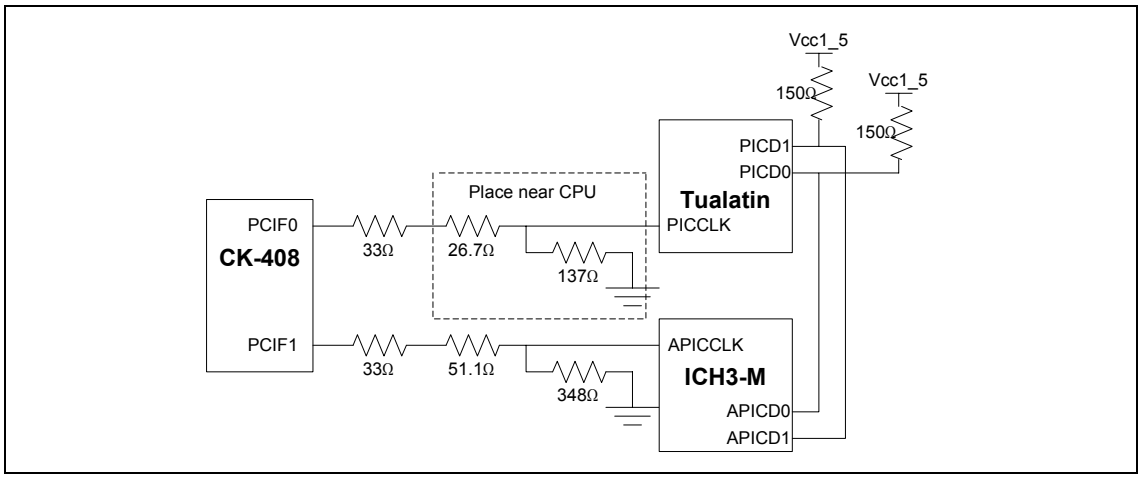
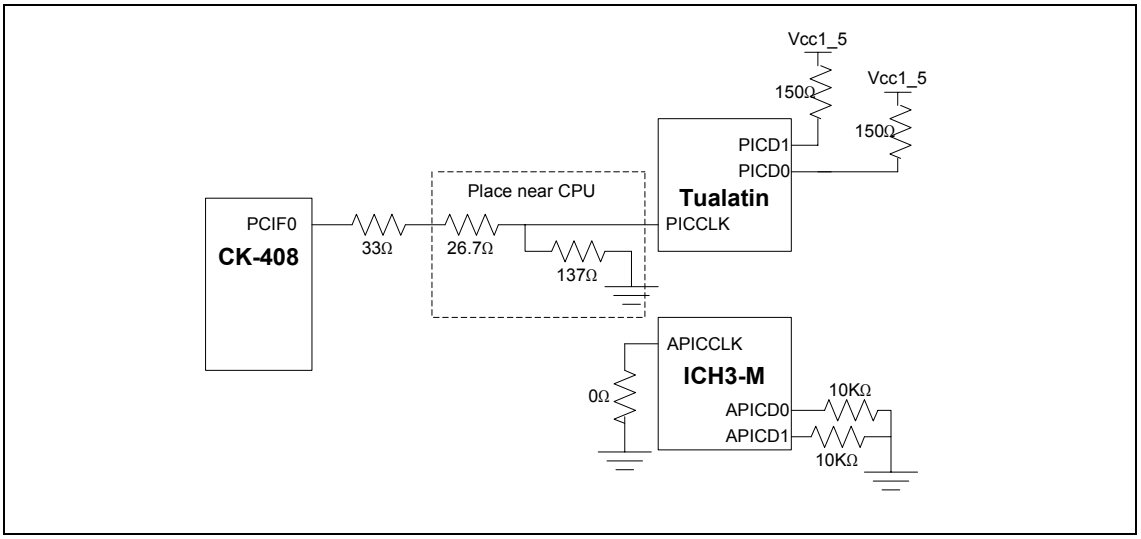


Figure 89. Minimum IOAPIC Disable Topology



12.5.2. GPIO

Checklist Items	Recommendations	Reason/Impact
GPIO Balls	**GPIO[7] & [5:0]:** • These balls are in the Main Power Well. Pull-ups must use the $V_{CC}3\_3$ plane. • Unused core well inputs must be pulled up to $V_{CC}3\_3$. • GPIO[1:0] can be used as REQ[B:A]#. • GPIO[1] can be used as PCI REQ[5]#. • GPIO[5:2] can be used as PIRQ[H:E]#. • These signals are 5-V tolerant.	*Ensure ALL unconnected signals are OUTPUTS ONLY!*
	GPIO[8] & [13:11]: • These balls are in the Resume Power Well. Pull-ups go to V_{CC}Sus3_3 plane. • Unused resume well inputs must be pulled up to V_{CC}Sus3_3. • These are the only GPIs that can be used as ACPI compliant wake events. • These signals are not 5V tolerant. • GPIO[11] can be used as SMBALERT#.	These are the only GPI signals in the resume well with associated status bits in the GPE1_STS register. Main power well GPIOs are 5 V tolerant, except for GPIO[43:32]. Resume power well GPIOs are not 5 V tolerant.
	GPIO[24:16]: • Fixed as output only. Can be left NC. • In Main Power Well ($V_{CC}3\_3$). • GPIO[17:16] can be used as GNT[B:A]#. • GPIO[17] can be used as PCI GNT[5]#. • STP_PCI#/GPIO[18] – used in mobile as STP_PCI# only. • SLP_S1#/GPIO[19] - used in mobile as SLP_S1# only. • STP_CPU#/GPIO[20] - used in mobile as STP_CPU# only. • C3_STAT#/GPIO[21] - used in mobile as C3_STAT# only. • CPUPERF#/GPIO[22] - open drain signal. Used in mobile as CPUPERF# only. • SSMUXSEL/GPIO[23] - used in mobile as SSMUXSEL only.	

	GPIO[28,27,25,24]: • I/O balls. Default as outputs. Can be left NC. • CLKRUN#/GPIO[24] • From resume power well (V_{CC}Sus3_3). (Note: use pull-up to V_{CC}3_3 if this signal is pulled-up)	
	GPIO[43:32]: I/O balls. From main power well (V_{CC}3_3). Default as outputs when enabled as GPIOs.	

NOTE: GPIO Inputs cannot be left floating.

12.5.3. AGP Busy/Stop Design Requirements

AGP Busy/Stop design requirements

Signal	System Pull-up/ Pull-down	Ω	Notes	✓
AGPBUSY#	Pull up to switched Vcc3_3	10 KΩ	This ICH3-M signal requires a pull-up to the switched 3.3-V rail (the 3.3-V power rail which will be powered OFF during S3). This applies to designs with graphics support either through an external AGP controller or GMCH-M internal graphics. When an external AGP controller is used, this ICH3-M signal must be connected to the AGP_BUSY# output of the external AGP Graphics Controller. Whenn 830M internal graphics is used, this ICH3-M signal must be connected to the AGP_BUSY# output of the GMCH-M. Please consult Intel 830M Family CRB schematics pg 9, 16, 19 and 21 for reference.	
C3_STAT#	No pull-up/ pull-down required. See Notes		When an external AGP device is enabled, this signal must be connected from ICH3-M to the external AGP Graphics Controller for STP_AGP# signal implementation. Please consult Intel 830M Family CRB schematics pg 16 and 19 for reference. This signal is not used by the GMCH-M internal graphics.	
SUS_STAT#	No pull-up/ pull-down required. See Notes		When an external AGP device is enabled, this signal must be connected from ICH3-M to the external AGP Graphic Controller if the AGP device is designed to use this signal. Assertion of this ICH3-M signal indicates that the system will be entering one of the S1-S5 low-power states, and that the platform clocks (including the AGP clock) will soon stop toggling. This signal can be monitored by devices with memory that need to switch from normal refresh to suspend refresh mode. It can also be used as an indication that the peripherals should isolate their outputs that may be going to powered-off planes. Please consult Intel 830M Family CRB schematics pg 16, 19, 32, 34, and 36 for reference. This signal is not used by the GMCH-M internal graphics.	

NOTE: Please also consult Intel for the latest AGP Busy and Stop signal specification.

12.5.4. (SM-Bus) System Management Interface

ICH3-M System Management Interface – Resistor Recommendations				
Signal	**System Pull-up/ Pull-down**	**Ω**	**Notes**	**✓**
INTRUDER#	Pull-up to VccRTC	8 K-22 KΩ	RTC well input requires pull-up to reduce leakage from coin cell battery in G3.	
SMLINK[1:0]	Pull-up to V3ALWAYS	4.7 KΩ	Require external pull-up resistors. Pull-up value is determined by bus section characteristics. Additional circuitry may be required to connect high and low powered sections. Resistor change for faster rise times and to ensure timings are within specification. Value or pull-up resistors is also determined by line load. Typical value used is 4.7 K - 8.2 KΩ. Tie to SMBus signals for SMBus compliance.	
SMBALERT#/ GPIO[11]	Pull-up to V3ALWAYS	10 KΩ		
SMBCLK, SMBDATA	Pull-up to V3ALWAYS	See Notes	Require external pull-up resistors. Pull-up value is determined by bus section characteristics. Additional circuitry may be required to connect high and low powered sections. Resistor change for faster rise times and to ensure timings are within specification. Value or pull-up resistors is also determined by line load. Typical value used is 8.2 KΩ. Tie to SMLink signals for SMBus compliance. See Intel 830M Family CRB Sch. p21.	

12.5.5. AC ’97 Interface

ICH3-M AC ’97 Interface – Resistor Recommendations					
Signal	**System Pull-up/ Pull-down**	**Ω**	**Series Damping**	**Notes**	**✓**
AC_BIT_CLK	No extra pull-down resistors required			The internal pull-down resistor is controlled by the AC’97 Global Control Register, ACLINK Shut Off bit: 1 = enabled 0 = disabled When no AC'97 devices are connected to the link, BIOS must set the ACLINK Shut Off bit for the internal keeper resistors to be ENABLED. At that point, pull-ups/pull-downs are NOT needed on ANY of the link signals.	
AC_SDIN[1:0]				Has integrated pull-down. No extra pull downs resistors are required. Intel 830M Family CRB Sch. uses 10KΩ pull-down. This is for adding termination for singal integrity to AC’97 Mobile connector. See CRB Schematics, page 24.	
AC_SDOUT	Requires jumper to R and pull-up to Vcc3_3. No stuff for default operation.	8.2 KΩ		Has internal pull-down 20 KΩ enabled only when AC_SHUT bit is set to 1. To properly detect a safe_mode condition, a strong pull-up will be required to over-ride internal pull-down.	
AC_SYNC			33Ω	Depends on actual strength of buffer.	

12.5.6. ICH3-M Power Management Interface

ICH3-M Power Management Interface – Resistor Recommendations					
Signal	**System Pull-up/ Pull-down**	**Ω**	**Series Damping**	**Notes**	**✓**
DPRSLPVR				External pull-up/down not required. Signal has integrated pull-down in ICH3-M.	
SLP_S3#, SLP_S5#				External pull-up/down not required. Signals driven by ICH3-M.	
LAN_RST#				Timing Requirement: Signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VccSus3_3 and VccSus1_8 have reached their nominal voltages. Intel 830M Family CRB Sch. uses 10 KΩ pull-down for PM_RSMRST#. See p34 **NOTE**: If ICH3-M LAN controller is NOT used, pull LAN_RST# down through a 10 KΩ resistor or connect directly to RSMRST#	
PWRBTN#				Has integrated pull-up of 18 KΩ – 42 KΩ.	
PWROK	Pull-down to GND	8K-22 KΩ		RTC well input requires pull-down to reduce leakage from coin cell battery in G3. Input must not float in G3. This signal should be connected to power monitoring logic and should go high no sooner than 10 ms after both Vcc3_3 and Vcc1_8 have reached their nominal voltages.	
RI#	Pull-up to V3ALWAYS	8.2 KΩ		Intel 830M Family CRB Sch. uses 10 KΩ. See p21 If this signal is enabled as a wake event, it is important to keep this this signal powered during a power loss event. If this signal goes low (active), when power returns the RI_STS bit will be set and the system will interpret that as a wake event.	
RSMRST#	Pull-down to GND	8 K-22 KΩ		RSMRST# is a RTC well input and requires pull-down to reduce leakage from coin cell battery in G3. Input must not float in G3. This signal should be connected to power monitoring logic and should go high no sooner than 10 ms after both Vcc3_3 and Vcc1_8 have reached their nominal voltages. Timing Requirement: See LAN_RST#	
STP_CPU#	Pull-up to Vcc3_3	10 KΩ		No stuff if DRCG is not used. See Intel 830M Family CRB Sch. p49.	
THRM#	Pull-up to Vcc3_3	8.2 KΩ		Pull-up required only if temperature sensor not used. Alternative system can be 2.7 KΩ to Vcc5. External pull-up/down not required if connecting to temperature sensor.	
VGATE	Pull-up to Vcc3_3	100 KΩ		See Intel 830M Family CRB Sch. p45.	

12.5.7. FWH/LPC Interface

ICH3-M FWH/LPC Interface – Resistor Recommendations				
Signal	**System Pull-up/Pull-down**	**Ω**	**Notes**	**✓**
LAD[3:0]/FWH[3:0],			ICH3-M integrates 24 KΩ pull-ups resistors on	

ICH3-M FWH/LPC Interface – Resistor Recommendations				
Signal	**System Pull-up/Pull-down**	**Ω**	**Notes**	**✓**
LDRQ[1:0]#			these signal lines.	
GPIO[7]	Pull-up to V3ALWAYS	10 KΩ	Intel 830M Family CRB uses GPIO[7] as LPC_PME#.	

12.5.8. USB Interface

ICH3-M USB Interface – Resistor Recommendations					
Signal	**System Pull-up/ Pull-down**	**Ω**	**Series Damping**	**Notes**	**✓**
OC[5:0]#	Pull-up to VccSus3_3	10 KΩ		Required pull-ups if not used. Inputs must not float. Intel 830M Family CRB Sch. pulls OC4# up to V3ALWAYS which is due to usage model. See Intel 830M Family CRB Sch. p22, 23	
USBP[5:0]N, USBP[5:0]P				Has integrated 15 K pull-downs. Output driver impedance of 45 Ω provided. Place near ICH3-M.	
USBRBIAS	Pull-down to GND	See Notes		**Resistor value for silicon stepping:** ICH3-M Ax: 33 KΩ ±1% ICH3-M B0 (QB 63 parts): 22.6 Ω ±1% ICH3-M B0 (QB 62 or SL5LF parts): 18.2 Ω ± 1% [BIOS workaround is also required for Sighting 17955]. Future ICH3-M steppings: 18.2 Ω ±1%	

12.5.9. Hub Interface

12.5.9.1. Hub Interface Resistor Recommendations

ICH3-M Hub Interface – Resistor Recommendations				
Signal	**System Pull-up/Pull-down**	**Ω**	**Notes**	**✓**
HI[10:0]			Route signals with 5 on 10 trace/ space routing for HI[7:0] and 15 mil spacing from other signals. In order to breakout of the GMCH-M and ICH3-M, 5 on 5 trace/space routing can be used within 300mils of packages and 5 on 10 thereafter. HI[7:0] must match within ± 0.2" of HI_STB and HI_STB# signals. Refer to Intel 830 Chipset Family Design Guide Sec 9.2.	
HICOMP	Pull-down to GND	36.5Ω ±1%	Place within 0.5 inches of ICH3-M pad using thick trace; Should be 2/3 board impedance. ZCOMP no longer supported.	

NOTE: Default tolerance for resistors is ±5% unless otherwise specified.

12.5.9.2. Decoupling Recommendations

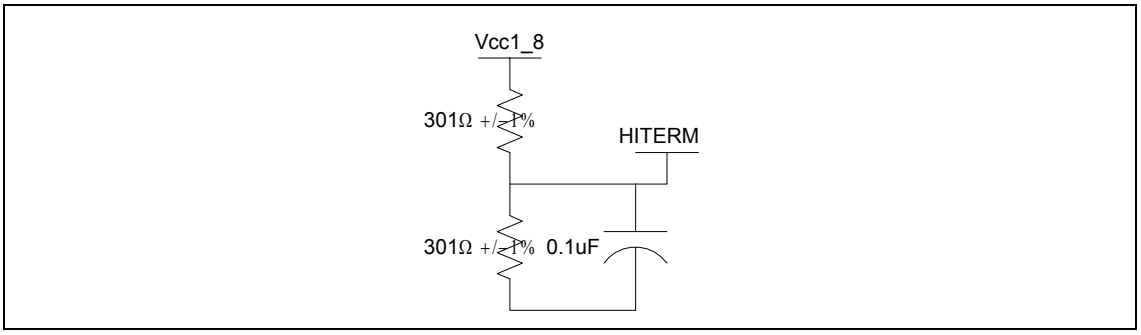
ICH3-M Hub Interface - Decoupling Recommendations[1]					
Signal	**Configuration**	**F**	**Qty**	**Notes**	**✓**
HITERM, HIREF	Pull-down to GND	0.01 µF	1 ea.		

12.5.9.3. Reference Voltage Dividers

ICH3-M Hub Interface – Reference Voltage Dividers[1]				
Signal	**System Pull-up/Pull-down**	**Ω**	**Notes**	**✓**
HITERM	Voltage divider w/ bottom resistor parallel to RC in series (0.1 µF and 0 Ω)	301 Ω ±1% (for both)	Place divider pair in middle of bus; Range for voltage divider resistors: 100 Ω – 1 KΩ; Refer to Intel 830M Family CRB Sch. p18 or Fig. 8-3	

NOTE: [1]All decoupling guidelines are recommendations based on our reference board design. Customers will need to take their layout, and PCB board design into consideration when deciding on their overall decoupling solution.

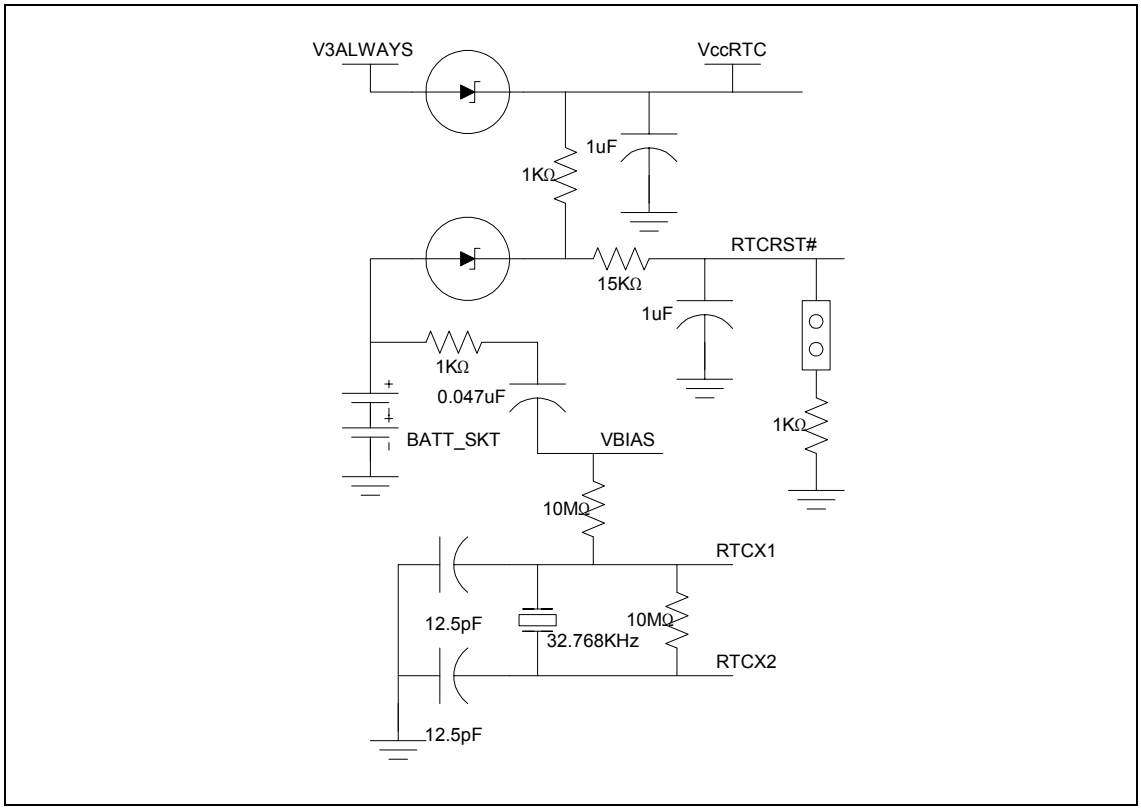
Figure 90. Hub Interface Termination Voltage



12.5.10. RTC Circuitry

ICH3-M RTC Circuitry Topology Recommendations				
Signal	**System Pull-up/Pull-down**	**Ω**	**Notes**	**✓**
RTCX1, RTCX2	Connect a 32.768 KHz crystal oscillator across these pins with a 10 MΩ resistor and use 12.5pF decoupling caps at each signal.	10 MΩ	Intel 830M Family CRB implements 10 pF caps. See Figure 89 or Intel 830M Family CRB Sch. p19 Circuitry is required since the new RTC oscillator is sensitive to step voltage changes in VCCRTC and VBIAS. A negative step on power supply of more than 100 mV will temporarily shut off the oscillator for hundreds of milliseconds.	
VBIAS	Connect 10 MΩ across to RTCX1 and 0.047 µF cap in series with 1 KΩ going to VBAT	10 MΩ 1 KΩ	Cap for noise immunity. See Figure 89 or Intel 830M Family CRB Sch. p19.	

Figure 91. RTC Circuitry



12.5.11. LAN Interface

ICH3-M LAN Interface Recommendations				
Signal	**System Pull-up/Pull-down**	**Ω**	**Notes**	**✓**
LAN_CLK	See Notes		Connect to LAN_CLK on Platform LAN Connect Device. If LAN interface not used, leave unconnected (NC).	
LAN_RXD[2:0]	See Notes		Connect to LAN_RXD on Platform LAN Connect Device. ICH3-M contains integrated 9 KΩ pull-up resistors on interface. If LAN interface not used, leave unconnected (NC).	
LAN_TXD[2:0], LAN_RSTSYNC	See Notes		Connect to LAN_TXD on Platform LAN Connect Device. If LAN interface not used, leave unconnected (NC).	

12.5.12. IDE Interface

ICH3-M IDE Interface – Resistor Recommendations					
Signal	**System Pull-up/ Pull-down**	**Ω**	**Series Damping**	**Notes**	**✓**
IDERST#	None		33 Ω	IDERST# should be buffered from PCIRST# signal.	
PDD[15:0], SDD[15:0]	None			No extra series termination resistors or other pull-ups/pull-downs are required. These signals have integrated series resistors. PDD7/SDD7 does not require a 10 KΩ pull-down resistor. **NOTE:** Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω but can range from 31 Ω to 43 Ω. Refer to ATA ATAPI-4 specification.	
PDIOW#, PDIOR#, PDDACK#, PDA[2:0], PDCS1#, PDCS3#, SDIOW#, SDIOR#, SDDACK#, SDA[2:0], SDCS1#, SDCS3#	None			No extra series termination resistors. Pads for series resistors can be implemented should the system designer have signal integrity concerns. These signals have integrated series resistors. **NOTE:** Simulation data indicates that the integrated series termination resistors are a nominal 33 but can range from 31 to 43 .	
PDREQ, SDREQ	None			No extra series termination resistors. No pull-down resistors needed. These signals have integrated series resistors in the ICH3-M. These signals have integrated pull-down resistors in the ICH3-M.	
IRQ14, IRQ15	Pull-up to Vcc3_3	8.2 KΩ - 10 KΩ		No extra series termination resistors. Open drain outputs from drive.	
PIORDY, SIORDY	Pull-up to Vcc3_3	4.7 KΩ		These signals have integrated series resistors in the ICH3-M.	

NOTE: The maximum trace length from the ICH3-M to the ATA connector is 8 inches.

12.5.13. Miscellaneous Signals

ICH3-M Miscellaneous Signals					
Signal	**System Pull-up/ Pull-down**	**Ω**	**Series Damping**	**Notes**	**✓**
BATLOW#	Pull-up to V3ALWAYS	10 KΩ		Must not float if unused. See Intel 830M Family CRB Sch. p34.	
RTC_RST#	Pull-down to GND See Notes	1 KΩ		CMOS setting. No pull-down required for normal operation. Use shunt to clear settings. Signal delay is 10-20 ms. See Intel 830M Family CRB Sch. p19 or Figure 89.	
SPKR	See Notes			SPKR is a strapping option for the TCO Timer Reboot function and is sampled on the rising edge of PWROK. An integrated weak pull-down is enabled only at boot/reset. Status of strap is readable via the NO_REBOOT bit (D31:F0, Offset D4h, bit 1). 1 = disabled 0 = enabled (normal operation) To disable, a jumper can be populated to pull SPKR high. Value of pull-up must be such that the voltage divider output caused by the pull-up, effective impedance of speaker and codec circuit, and internal pull-down will be read as logic high (0.5 * Vcc3_3 to Vcc3_3 + 0.5).	

12.5.14. Decoupling Recommendations

ICH3-M – Decoupling Recommendations[1]					
Signal	**Configuration**	**F**	**Qty**	**Notes**	**✓**
Vcc1_5	Pull-down to GND	0.1 µF 1 µF_16 V	2 1	See Intel 830M Family CRB Sch. p20	
Vcc1_8	Pull-down to GND	0.1 µF 47 pF	5 2		
V1-8ALWAYS	Pull-down to GND	0.1 µF	3	Locate one cap within 200 mils of B23 and C23	
VccSus1_8	Pull-down to GND	0.1 µF	2		
Vcc3_3	Pull-down to GND	0.1 µF 47 pF	13 5		
V3ALWAYS	Pull-down to GND	0.1 µF	8		
VccSus3_3	Pull-down to GND	0.1 µF 47 pF_16 V	2 1		
V5REF[2:1]	See Section 11.1.5 for complete guidelines	0.1 µF 1 µF_16 V	2 1	Requires at least **1** 0.1 µF decoupling cap. (Intel 830 chipset CRB uses **2** 0.1 µF and **1** µF_16 V) V5REF is the reference voltage for 5-V tolerant inputs in the ICH3-M. Tie to balls V5REF[2:1]. V5REF must be powered up before Vcc3_3, or after Vcc3_3 within 0.7 V. Also, V5REF must power down after Vcc3_3, or before Vcc3_3 within 0.7 V.	
V5REF_Sus[2:1]	See Section 11.1.5 for complete guidelines	0.1 µF	1	Requires **1** 0.1 µF decoupling cap. V5REF_SUS is the reference voltage for some 5 V tolerant inputs in the Intel ICH3-M (USB data and over-current signals). Tie to balls V5REF_Sus[2:1]. V5REF_Sus must be powered up before VccSus3_3, or after VccSus3_3 within 0.7 V. Also, V5REF_Sus must power down after VccSus3_3, or before VccSus3_3 within 0.7 V.	
VccLan3_3[1:0]	Connect to +V3			Signal MUST be powered during S0 and S1 states even if ICH3-M LAN controller is NOT used	
VccLan1_8[2:0]	Connect to +V1_8			Signal MUST be powered during S0 and S1 states even if ICH3-M LAN controller is NOT used.	

12.5.15. Reference Voltage Dividers

ICH3-M – Reference Voltage Dividers[1]				
Signal	**System Pull-up/Pull-down**	**Ω**	**Notes**	**✓**
V5REF[2:1]	Pull-up to Vcc5	1 KΩ	See Intel 830M Family CRB Sch. p20	

NOTE: [1]All decoupling guidelines are recommendations based on our reference board design. Customers will need to take their layout, & PCB board design into consideration when deciding on their overall decoupling solution.

12.6. USB Checklist

12.6.1. Resistor Recommendations

USB – Resistor Recommendations					
Signal	**System Pull-up/Pull-down**	**Ω**	**Series Damping**	**Notes**	**✓**
USBPWRCONN [D:A]	LC Pi filter – one 0.1 µF, one 150 µF_16 V, and one ferrite bead			Both caps on Pin 1 of ferrite bead. Optimal decoupling acheived with 150 µF cap on connector side of ferrite bead. See Intel 830M Family CRB Sch. p22-23.	

NOTE: Default tolerance for resistors is ±5% unless otherwise specified.

12.6.2. Decoupling Recommendations

USB – Decoupling Recommendations[1]					
Signal	**Configuration**	**F**	**Qty**	**Notes**	**✓**
BT_PWR	Pull-down to GND	0.01 µF 150 µF_16 V	1 1		
V5_USB[2:1]	Pull-down to GND	0.01 µF	1 ea.		

NOTE: 1All decoupling guidelines are recommendations based on our reference board design. Customers will need to take their layout, & PCB board design into consideration when deciding on their overall decoupling solution.

12.7. AC '97 Checklist

12.7.1. Resistor Recommendations

AC '97 – Resistor Recommendations					
Signal	**System Pull-up/Pull-down**	**Ω**	**Series Damping**	**Notes**	**✓**
Conn.Pins: [7,5] (AC97_AUXA_ [L,R]), [13,11] (AC97_CD_ [L,R])	RC filter – R pull-down to GND and 1 µF cap in series	5.6 KΩ	5.6 KΩ	See Intel 830M Family CRB Sch. p24.	

NOTE: Default tolerance for resistors is ±5% unless otherwise specified.

12.7.2. Decoupling Recommendations

AC '97 – Decoupling Recommendations[1]					
Signal	**Configuration**	**F**	**Qty**	**Notes**	**✓**
VccSus3_3	Pull-down to GND	0.01 µF	1		
V3_MDC	Pull-down to GND	0.01 µF	1		
V3A_MDC	Pull-down to GND	0.01 µF	1		
V5_MDC	Pull-down to GND	0.01 µF	1		

NOTE: [1]All decoupling guidelines are recommendations based on our reference board design. Customers will need to take their layout, & PCB board design into consideration when deciding on their overall decoupling solution.

12.8. FWH Checklist

12.8.1. Resistor Recommendations

FWH – Resistor Recommendations					
Signal	**System Pull-up/Pull-down**	**Ω**	**Series Damping**	**Notes**	**✓**
FGPI[4:0]	Pull-down to GND	10 KΩ			
IC	Pull-down to GND	10 KΩ			
INIT#	See Note	10 KΩ		Depends on FWH used.	

NOTE: Default tolerance for resistors is ±5% unless otherwise specified.

12.8.2. Decoupling Recommendations

FWH – Decoupling Recommendations[1]					
Signal	**Configuration**	**F**	**Qty**	**Notes**	**✓**
Vcc3_3	Pull-down to GND	0.01 µF	4		
		10 µF_10 V	1		

NOTE: [1]All decoupling guidelines are recommendations based on our reference board design. Customers will need to take their layout, & PCB board design into consideration when deciding on their overall decoupling solution.

12.9. LAN / HomePNA Checklist

12.9.1. LAN Interface (82562ET / 82562EM)

12.9.1.1. Resistor Recommendations

LAN – Resistor Recommendations					
Signal	**System Pull-up/Pull-down**	**Ω**	**Series Damping**	**Notes**	**✓**
ACTLED			470Ω		
CT[3:2]	Pull-down to GND	75 Ω ± 1%		From LAN_MAGNETICS component.	
ISOL_TCK, ISO_TI, ISOL_EX, TESTEN	Pull-up to VccSus3_3	10 KΩ		All 4 signals can be pulled-up with a common resistor. See Intel 830M Family CRB Sch. p38.	
RBIAS100	Pull-down to GND	619 Ω ±1%			
RBIAS10	Pull-down to GND	549 Ω ±1%			
RDP, RDN		100 Ω ±1%		Crossover resistor.	
SPDLED	Pull-up to VccSus3_3	470 Ω			
TDP, TDN		100 Ω ±1%		Crossover resistor. See Intel 830M Family CRB Sch. p38.	
X1, X2				Connect to 25-MHz crystal.	
[16:15,13:12]	Pull-down to GND	75 Ω ± 1%		From RJ45-USB Conn.	
[20]	Pull-up to VccLAN3_3	470 Ω		From LAN_MAGNETICS component.	

NOTE: Default tolerance for resistors is ±5% unless otherwise specified.

12.9.1.2. Decoupling Recommendations

LAN – Decoupling Recommendations[1]					
Signal	**Configuration**	**F**	**Qty**	**Notes**	**✓**
CT1	Pull-down to GND	0.1 µF	1	From LAN_MAGNETICS component.	
VccLAN3_3	Pull-down to GND	0.1 µF 4.7 µF	4 2	See Intel 830M Family CRB Sch. p38.	
VccLAN_L3_3	Pull-down to GND	0.1 µF 4.7 µF	1 1	Supplies power to VccR pins of 82562ET/ 82562EM. See Intel 830M Family CRB Sch. p38.	
X1, X2	Pull-down to GND	22 pF	1		

NOTE: [1]All decoupling guidelines are recommendations based on our reference board design. Customers will need to take their layout, & PCB board design into consideration when deciding on their overall decoupling solution.

12.9.2. HomePNA

12.9.2.1. Resistor Recommendations

HomePNA – Resistor Recommendations					
Signal	**System Pull-up/Pull-down**	**Ω**	**Series Damping**	**Notes**	**✓**
IREF	Pull-down to GND	619 Ω ± 1%			
LEDA_L, LEDL_L	Pull-up to VccLAN3_3	470 Ω			
PHAD3/DFT3/ CL_L	Pull-up to VccLAN3_3	10 KΩ		Can be same shared resistor as ISOL_TI, _TCK, _EX, and TESTEN. See Intel 830M Family CRB Sch. p38.	
PHAD4/GPSI	Pull-down to GND	10 KΩ			
RX_TX_P, RX_TX_N	Pull-up to V3_L_D_PNA	51.1 Ω ±1%		V3_L_D_PNA is the pull-up rail for the RX_TX_P and RX_TX_N pins of 82562EH.	
TEST_EN	Pull-down to GND	1 KΩ			
TX_EN, MDC, MDIO, ISOLATE, HMII/JORD	Pull-down to GND	1 KΩ			
XO			121 Ω ± 1%	With crossover resistor 10 KΩ to XI. Connected to 20-MHz crystal. See Intel 830M Family CRB Sch. p39.	

NOTE: Default tolerance for resistors is ±5% unless otherwise specified.

12.9.2.2. Decoupling Recommendations

HomePNA – Decoupling Recommendations[1]					
Signal	**Configuration**	**F**	**Qty**	**Notes**	**✓**
IREF	Pull-down to GND	0.1 µF	1		
XI	Pull-down to GND	82 pF	1		
XO	Pull-down to GND	120 pF	1		

NOTE: [1]All decoupling guidelines are recommendations based on our reference board design. Customers will need to take their layout, & PCB board design into consideration when deciding on their overall decoupling solution.

12.10. Appendix

12.10.1. Intel 830MP Recommendations for Unconnected Interfaces

Intel 830MP (Performance Discrete) Recommendations			
GMCH-M Signal	**Ball #**	**External Graphics 830MP**	✓
DVOA			
DVOA_FLD/STL	AE22	Pull-down required	
DVOA_CLKINT	AD20	Pull-up required	
DVOA_INTR#	AE21	Pull-up required	
DVOA_RCOMP	AC22	Pull-down required	
DDC1CLK DDC1DATA	AE27 AD27	Pull-up required	
DDC2CLK DDC2DATA	AE26 AD26	Pull-up required	
I2CDATA I2CCLK	AC25 AD25	Pull-up required	
CRT			
RED GREEN BLUE	AF29 AG29 AH28	NC	
RED# GREEN# BLUE#	AF28 AG28 AH27	NC	
REFSET	AJ27	NC	
VSYNC HSYNC	AE29 AD28	NC	
DREFCLK	AC19	Pull down required	
VCCA_DPLL[1] VCCA_DPLL[0]	F25 AC20	Pull-up to VTT required	
Reserved Signals			
LM_CMD [Reserved]	AH7	NC	
CFM [Reserved]	AJ16	NC	
CFM# [Reserved]	AH16	NC	
CTM [Reserved]	AH15	Pull-down required	
CTM# [Reserved]	AJ15	Pull-down required	
GM_GCLK [Reserved]	AG6	NC	
GM_RCLK [Reserved]	AJ6	NC	
RAMREF[1] [Reserved] RAMREF[0] [Reserved]	AE14 AD14	No RC filter. Voltage divider need; 1% resistors not required	
SCK [Reserved]	AF7	NC	
SIO [Reserved]	AJ7	NC	

12.10.2. Intel 830MG Recommendations for Unconnected Interfaces

GMCH-M – (Integrated Value) Recommendations			
GMCH-M Signal	**Ball #**	**Internal Graphics – UMA**	**✓**
DVOA			
DVOA_FLD/STL	AE22	Pull-down required	
DVOA_CLKINT	AD20	Pull-up required	
DVOA_INTR#	AE21	Pull-up required	
DVOA_RCOMP	AC22	Pull-down required	
DDC1CLK DDC1DATA	AE27 AD27	Pull-up required	
DDC2CLK DDC2DATA	AE26 AD26	Pull-up required	
I2CDATA I2CCLK	AC25 AD25	Pull-up required	
DVOBC			
DVOBC_CLKINT	M25	Pull-up required	
DVOB_FLD/STL	N26	Pull-down required	
DVOC_FLD/STL	Y29	Pull-down required	
DVO[C]_CLK DVO[B]_CLK	U29 L29	NC	
DVO[C]_CLK# DVO[B]_CLK#	U28 L28	NC	
AGP_BUSY#	AC24	Pull-up required	
DVOBC_RCOMP	K24	Pull-down required	
M_I2C_DATA	R28	Pull-up required	
M_DDC1_DATA	R29	Pull-up required	
M_I2C_CLK	P26	Pull-up required	
M_DDC1_CLK	P27	Pull-up required	
Reserved Signals			
LM_CMD [Reserved]	AH7	NC	
CFM [Reserved]	AJ16	NC	
CFM# [Reserved]	AH16	NC	
CTM [Reserved]	AH15	Pull-down required	
CTM# [Reserved]	AJ15	Pull-down required	
GM_GCLK [Reserved]	AG6	NC	
GM_RCLK [Reserved]	AJ6	NC	
RAMREF[1] [Reserved] RAMREF[0] [Reserved]	AE14 AD14	No RC filter; Voltage divider needed; 1% resistors not required	

GMCH-M – (Integrated Value) Recommendations			
GMCH-M Signal	**Ball #**	**Internal Graphics – UMA**	**✓**
RQ[7] [Reserved] RQ[6] [Reserved] RQ[5] [Reserved] RQ[4] [Reserved] RQ[3] [Reserved] RQ[2] [Reserved] RQ[1] [Reserved] RQ[0] [Reserved]	AJ14 AG14 AJ13 AG13 AH13 AG12 AJ12 AG11	NC	
SCK [Reserved]	AF7	NC	
SIO [Reserved]	AJ7	NC	

12.10.3. Intel 830M Recommendations for Unconnected Interfaces

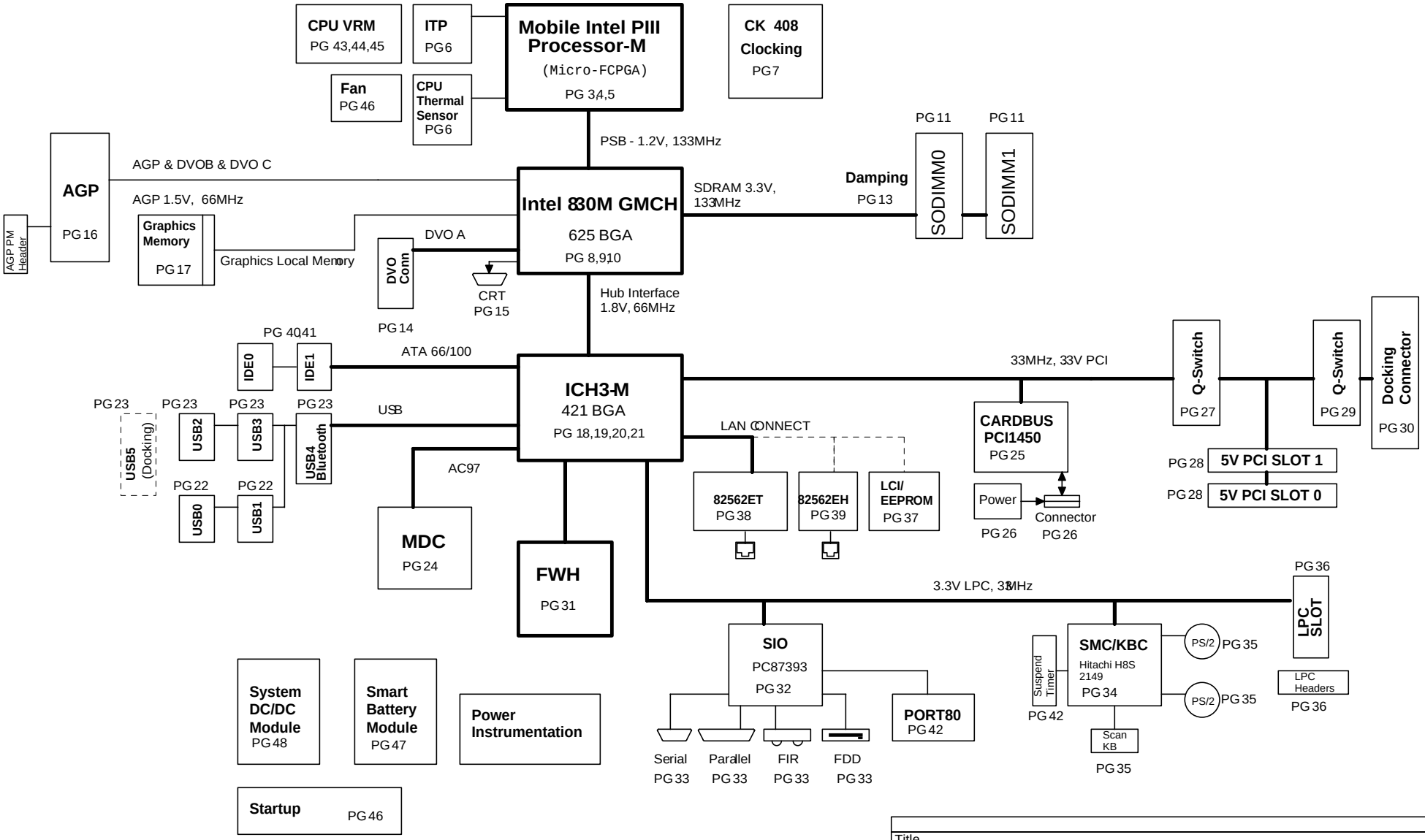
GMCH-M – (Integrated Performance) Recommendations				
GMCH-M Signal	**Ball #**	**External Graphics**	**Internal Graphics – UMA**	**✓**
DVOA				
DVOA_FLD/STL	AE22	Pull-down required	Pull-down required	
DVOA_CLKINT	AD20	Pull-up required	Pull-up required	
DVOA_INTR#	AE21	Pull-up required	Pull-up required	
DVOA_RCOMP	AC22	Pull-down required	Pull-down required	
DDC1CLK DDC1DATA	AE27 AD27	Pull-up required	Pull-up required	
DDC2CLK DDC2DATA	AE26 AD26	Pull-up required	Pull-up required	
I2CDATA I2CCLK	AC25 AD25	Pull-up required	Pull-up required	
AGP				
AGP_BUSY#	AC24	Pull-up required	Pull-up required	
AGP_RCOMP)	K24	Pull-down required	Pull-down required	
DVOBC				
DVOBC_CLKINT	M25	Not Appliable	Pull-up required	
DVOB_FLD/STL	N26	Not Appliable	Pull-down required	
DVOC_FLD/STL	Y29	Not Appliable	Pull-down required	
DVO[C]_CLK DVO[B]_CLK	U29 N26	Not Appliable	NC	
DVO[C]_CLK# DVO[B]_CLK#	U28 L28	Not Appliable	NC	
AGP_BUSY#	AC24	Pull-up required	Pull-up required	
DVOBC_RCOMP	K24	Pull-down required	Pull-down required	
M_I2C_DATA	R28	Not Appliable	Pull-up required	
M_DDC1_DATA	R29	Not Appliable	Pull-up required	
M_I2C_CLK	P26	Not Appliable	Pull-up required	
DVO_DETECT	P28	Not Appliable	Pull-down required (330 ohm)	

GMCH-M – (Integrated Performance) Recommendations				
GMCH-M Signal	**Ball #**	**External Graphics**	**Internal Graphics – UMA**	✓
M_DDC1_CLK	P27	Not Appliable	Pull-up required	
DVOBC_CLKINT	M25	Not Appliable	Pull-up required	
CRT				
RED GREEN BLUE	AF29 AG29 AH28	NC	Not Appliable	
RED# GREEN# BLUE#	AF28 AG28 AH27	NC	Not Appliable	
REFSET	AJ27	NC	Not Appliable	
VSYNC HSYNC	AE29 AD28	NC	Not Appliable	
DREFCLK	AC19	Pull down required	Not Appliable	
VCCA_DPLL[1] VCCA_DPLL[0]	F25 AC20	Tie directly to VTT	Not Appliable	
Reserved Signals				
LM_CMD [Resreved]	AH7	NC	NC	
CFM [Reserved]	AJ16	NC	NC	
CFM# [Reserved]	AH16	NC	NC	
CTM [Reserved]	AH15	Pull-down required	Pull-down required	
CTM# [Reserved]	AJ15	Pull-down required	Pull-down required	
GM_GCLK [Reserved]	AG6	NC	NC	
GM_RCLK [Reserved]	AJ6	NC	NC	
RAMREF[1] [Reserved] RAMREF[0] [Reserved]	AE14 AD14	No RC flter. Voltage divider need; 1% resistors not required	No RC filter; Voltage divider needed; 1% resistors not required	
RQ[7] [Reserved] RQ[6] [Reserved] RQ[5] [Reserved] RQ[4] [Reserved] RQ[3] [Reserved] RQ[2] [Reserved] RQ[1] [Reserved] RQ[0] [Reserved]	AJ14 AG14 AJ13 AG13 AH13 AG12 AJ12 AG11	NC	NC	
SCK [Reserved]	AF7	NC	NC	
SIO [Reserved]	AJ7	NC	NC	

13. Customer Reference Board Schematics

See following pages for the customer reference board schematics.

Intel 830 Chipset Family
Customers Reference Board



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830 Chipset Family Customer Reference Platform

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

+VDC/+VDC_IN	Primary DC system power supply (7 to 21V)
+VCC/+VCC_H_CORE	Core voltage for CPU
+VTT/+VTT_CPU	1.2V switched power rail for CPU IO and GTL pullups
+V1-5S	1.5V switched power rail (off in S3-S5)
+V1-8ALWAYS	1.8V always on power rail
+V1-8	1.8V power rail (off in S4-S5)
+V1-8S	1.8V switched power rail (off in S3-S5)
+V2-5	2.5V power rail for Graphics Memory (off in S4-S5)
+V2-5S	2.5V switched power rail for Graphics Memory
+V3ALWAYS	3.3V always on power rail
+V3	3.3V power rail (off in S4-S5)
+V3S	3.3V switched power rail (off in S3-S5)
+V5	5.0V power rail (off in S4-S5)
+V5S	5.0V switched power rail (off in S3-S5)
+V12S	12.0V switched power rail (off in S3-S5)

PCI Devices

Device	IDSEL #	REQ/GNT #	Interrupts	PC/PCI
CardBus	AD25	2	C, D	A
Slot 0	AD22	3	C, D, A, B	A
Slot 1	AD20	0	B,A, C, D	A
Docking	AD28	4	B, C, D, A	B
AGP	(AD17 internal)		A, B	
LAN	(AD24 internal)			
USB	AD29			
Hub to PCI	AD30			
LPC bridge/IDE/AC97/SMBus	AD31			

Power States

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S5#	+V3ALWAYS	+V*	+V*S	Clocks
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	ON	ON	OFF	LOW
S4 (Suspend To Disk)	LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 / Soft OFF	LOW	LOW	LOW	ON	OFF	OFF	OFF

I^2C / SMB Addresses

Device	Address	Hex	Bus
SDRAM	1010 000x	A0	SMB_ICH
Clock Generator	1101 001x	D2	SMB_ICH
SO-MRIMM	1010 011x	A6	SMB_ICH
Thermal Diode	1001 110x	9C	SMB_THRM
Smart Battery	0001 011x	16	SMB_SB
Smart Battery Charger	0001 001x	12	SMB_SB
Smart Selector	0001 010x	14	SMB_SB
Internal use for Security			SMB_SC

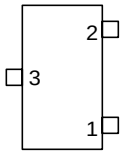
Net Name Suffix

\# = Active Low signal

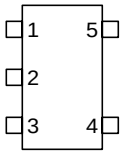
PCB Footprints

As seen from top

SOT-23



SOT23-5



Title: Notes and Annotations			
Size: A	Project:	Document Number:	Rev
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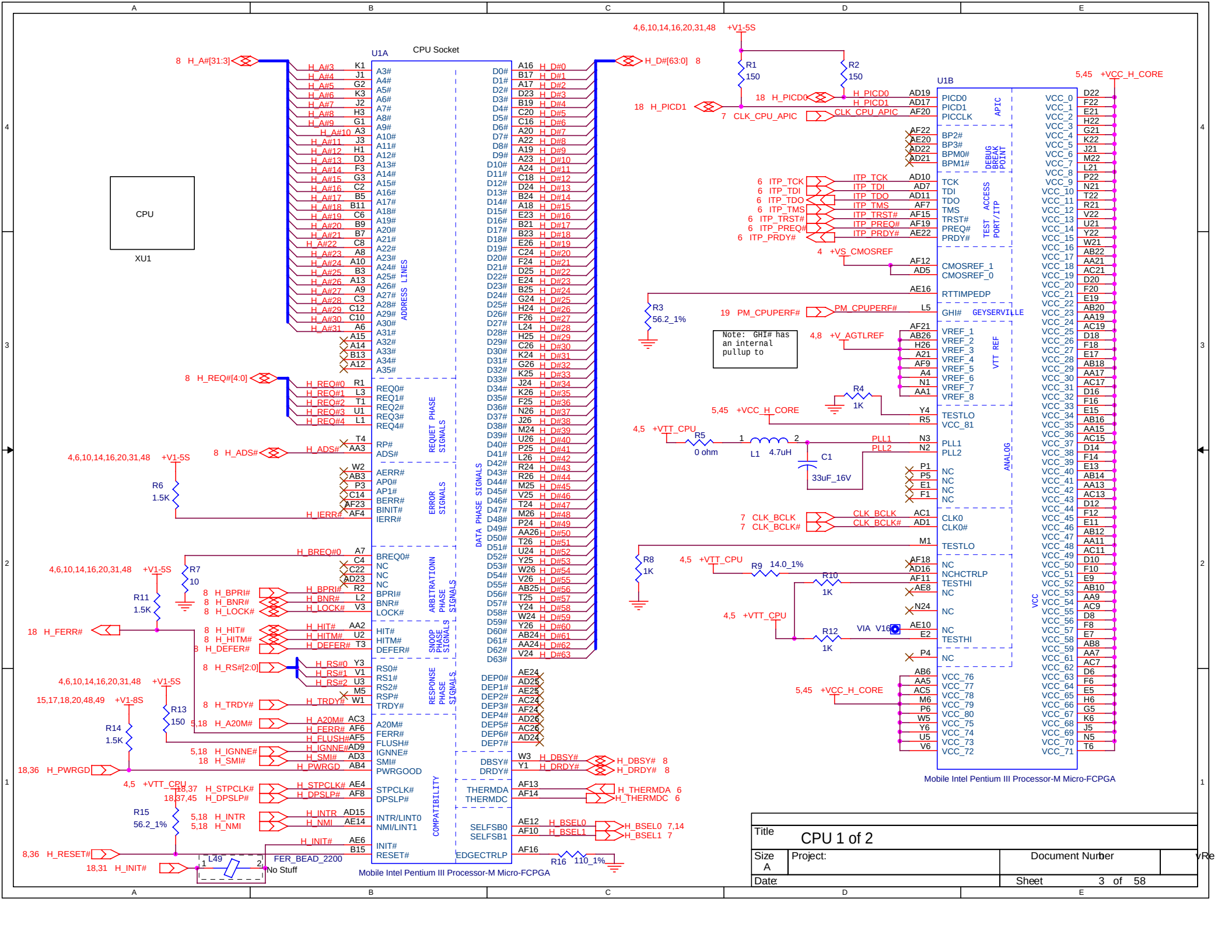
CPU Socket
U1A
CPU
XU1
U1B
Mobile Intel Pentium III Processor-M Micro-FCPGA
Mobile Intel Pentium III Processor-M Micro-FCPGA
Note: GHI# has an internal pullup to
Title
CPU 1 of 2
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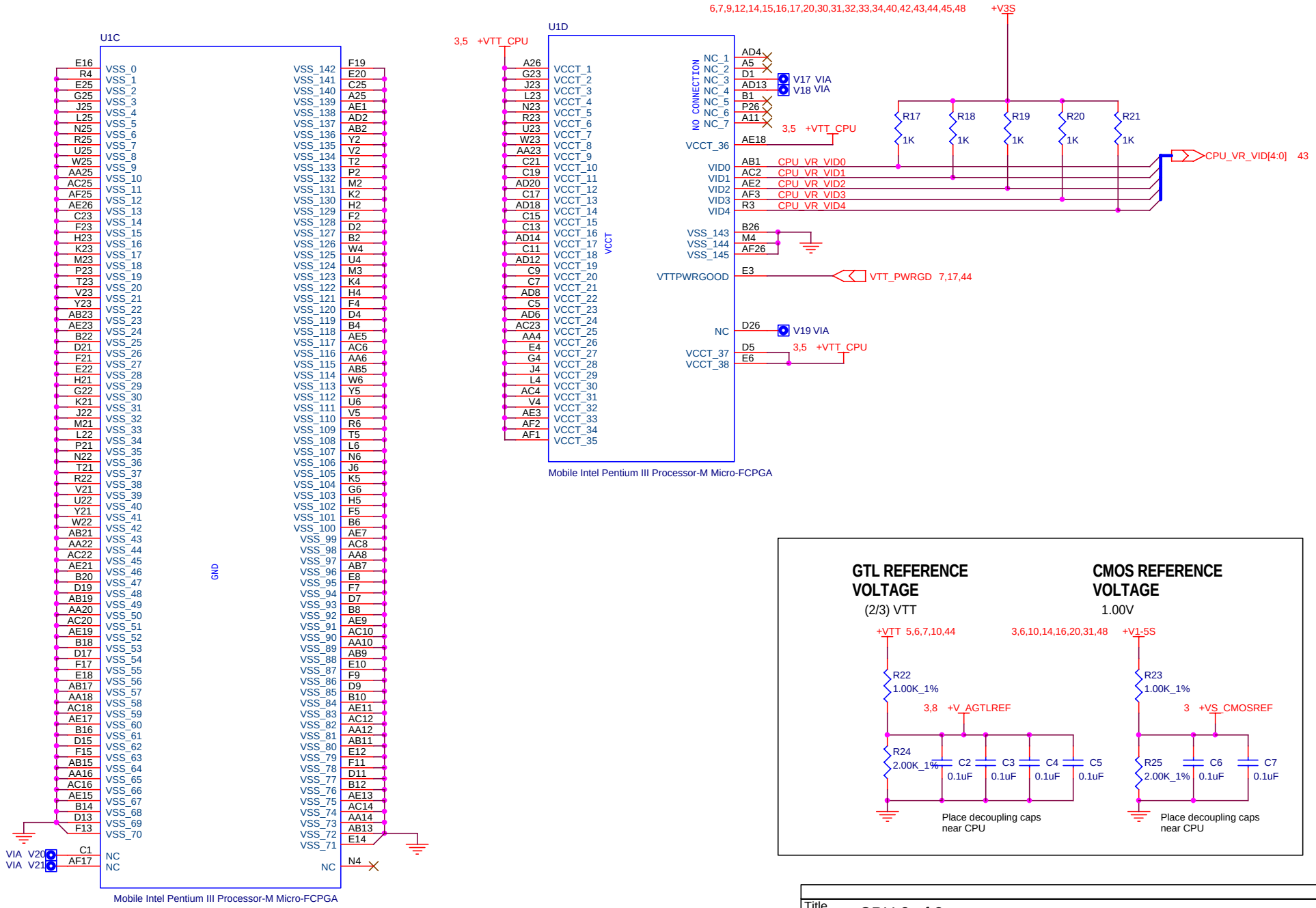
U1C
E16 R4 E25 G25 J25 L25 N25 R25 U25 W25 AA25 AC25 AF25 AE26 C23 F23 H23 K23 M23 P23 T23 V23 Y23 AB23 AE23 B22 D21 F21 E22 H21 G22 K21 J22 M21 L22 P21 N22 T21 R22 V21 U22 Y21 W22 AB21 AA22 AC22 AE21 B20 D19 AB19 AA20 AC20 AE19 B18 D17 F17 E18 AB17 AA18 AC18 AE17 B16 D15 F15 AB15 AA16 AC16 AE15 B14 D13 F13
VSS_0 VSS_1 VSS_2 VSS_3 VSS_4 VSS_5 VSS_6 VSS_7 VSS_8 VSS_9 VSS_10 VSS_11 VSS_12 VSS_13 VSS_14 VSS_15 VSS_16 VSS_17 VSS_18 VSS_19 VSS_20 VSS_21 VSS_22 VSS_23 VSS_24 VSS_25 VSS_26 VSS_27 VSS_28 VSS_29 VSS_30 VSS_31 VSS_32 VSS_33 VSS_34 VSS_35 VSS_36 VSS_37 VSS_38 VSS_39 VSS_40 VSS_41 VSS_42 VSS_43 VSS_44 VSS_45 VSS_46 VSS_47 VSS_48 VSS_49 VSS_50 VSS_51 VSS_52 VSS_53 VSS_54 VSS_55 VSS_56 VSS_57 VSS_58 VSS_59 VSS_60 VSS_61 VSS_62 VSS_63 VSS_64 VSS_65 VSS_66 VSS_67 VSS_68 VSS_69 VSS_70
GND
VSS_142 VSS_141 VSS_140 VSS_139 VSS_138 VSS_137 VSS_136 VSS_135 VSS_134 VSS_133 VSS_132 VSS_131 VSS_130 VSS_129 VSS_128 VSS_127 VSS_126 VSS_125 VSS_124 VSS_123 VSS_122 VSS_121 VSS_120 VSS_119 VSS_118 VSS_117 VSS_116 VSS_115 VSS_114 VSS_113 VSS_112 VSS_111 VSS_110 VSS_109 VSS_108 VSS_107 VSS_106 VSS_105 VSS_104 VSS_103 VSS_102 VSS_101 VSS_100 VSS_99 VSS_98 VSS_97 VSS_96 VSS_95 VSS_94 VSS_93 VSS_92 VSS_91 VSS_90 VSS_89 VSS_88 VSS_87 VSS_86 VSS_85 VSS_84 VSS_83 VSS_82 VSS_81 VSS_80 VSS_79 VSS_78 VSS_77 VSS_76 VSS_75 VSS_74 VSS_73 VSS_72 VSS_71
F19 E20 C25 A25 AE1 AD2 AB2 Y2 V2 T2 P2 M2 K2 H2 F2 D2 B2 W4 U4 M3 K4 H4 F4 D4 B4 AE5 AC6 AA6 AB5 W6 Y5 U6 V5 R6 T5 L6 N6 J6 K5 G6 H5 F5 B6 AE7 AC8 AA8 AB7 E8 F7 D7 B8 AE9 AC10 AA10 AB9 E10 F9 D9 B10 AE11 AC12 AA12 AB11 E12 F11 D11 B12 AE13 AC14 AA14 AB13 E14
C1 AF17
NC NC
N4 NC
VIA V20 VIA V21
Mobile Intel Pentium III Processor-M Micro-FCPGA
U1D
3,5 +VTT_CPU
A26 G23 J23 L23 N23 R23 U23 W23 AA23 C21 C19 AD20 C17 AD18 C15 C13 AD14 C11 AD12 C9 C7 AD8 C5 AD6 AC23 AA4 E4 G4 J4 L4 AC4 V4 AE3 AF2 AF1
VCCT_1 VCCT_2 VCCT_3 VCCT_4 VCCT_5 VCCT_6 VCCT_7 VCCT_8 VCCT_9 VCCT_10 VCCT_11 VCCT_12 VCCT_13 VCCT_14 VCCT_15 VCCT_16 VCCT_17 VCCT_18 VCCT_19 VCCT_20 VCCT_21 VCCT_22 VCCT_23 VCCT_24 VCCT_25 VCCT_26 VCCT_27 VCCT_28 VCCT_29 VCCT_30 VCCT_31 VCCT_32 VCCT_33 VCCT_34 VCCT_35
VCCT
NO CONNECTION
NC_1 NC_2 NC_3 NC_4 NC_5 NC_6 NC_7
AD4 A5 D1 AD13 B1 P26 A11
V17 VIA V18 VIA
3,5 +VTT_CPU
VCCT_36 AE18
VID0 VID1 VID2 VID3 VID4
AB1 AC2 AE2 AF3 R3
CPU_VR_VID0 CPU_VR_VID1 CPU_VR_VID2 CPU_VR_VID3 CPU_VR_VID4
6,7,9,12,14,15,16,17,20,30,31,32,33,34,40,42,43,44,45,48 +V3S
R17 R18 R19 R20 R21
1K 1K 1K 1K 1K
CPU_VR_VID[4:0] 43
VSS_143 VSS_144 VSS_145
B26 M4 AF26
VTTPWRGOOD E3
VTT_PWRGD 7,17,44
NC D26
V19 VIA
VCCT_37 VCCT_38 D5 E6
3,5 +VTT_CPU
Mobile Intel Pentium III Processor-M Micro-FCPGA
GTL REFERENCE VOLTAGE
(2/3) VTT
+VTT 5,6,7,10,44
R22 1.00K_1%
3,8 +V_AGTLREF
R24 2.00K_1%
C2 C3 C4 C5 0.1uF
Place decoupling caps near CPU
CMOS REFERENCE VOLTAGE
1.00V
3,6,10,14,16,20,31,48 +V1-5S
R23 1.00K_1%
3 +VS_CMOSREF
R25 2.00K_1%
C6 C7 0.1uF
Place decoupling caps near CPU
Title
CPU 2 of 2
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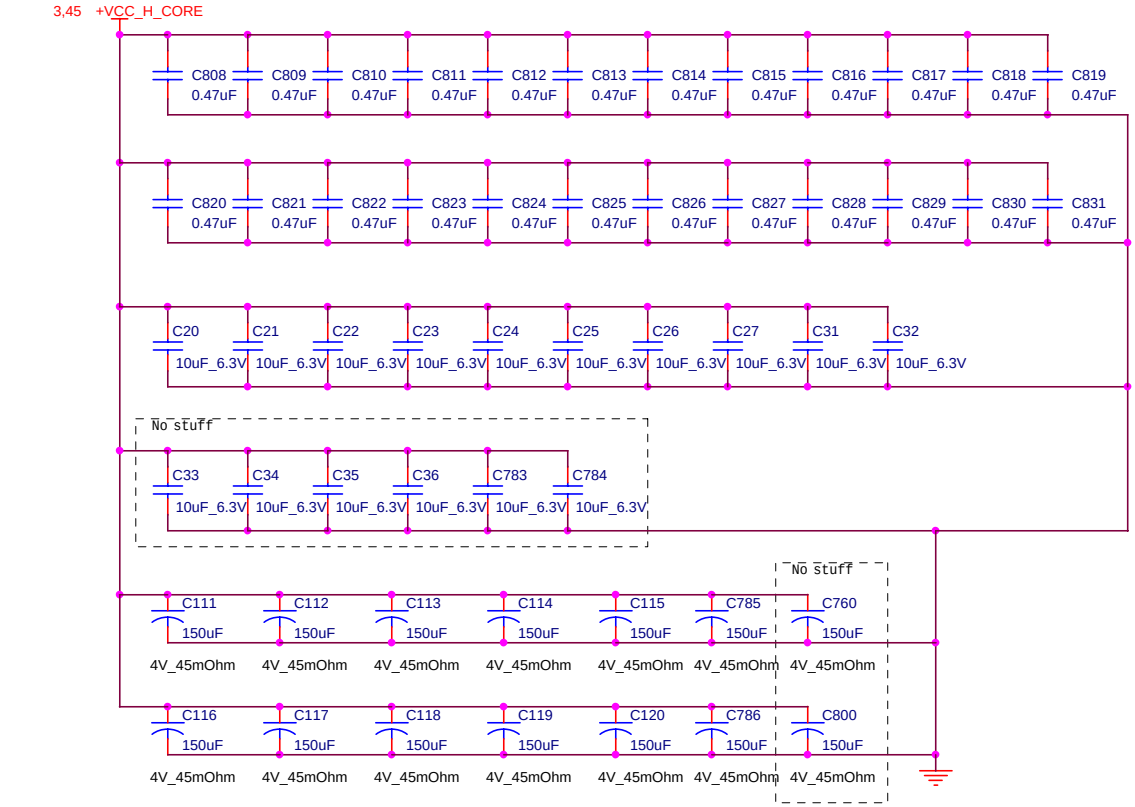
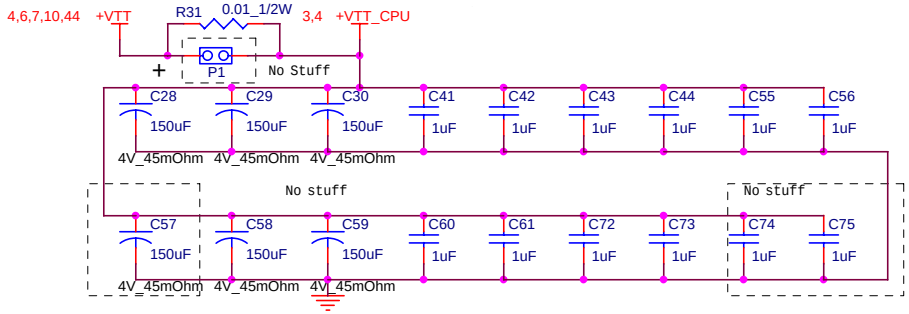
CPU DecouplingCapacitors



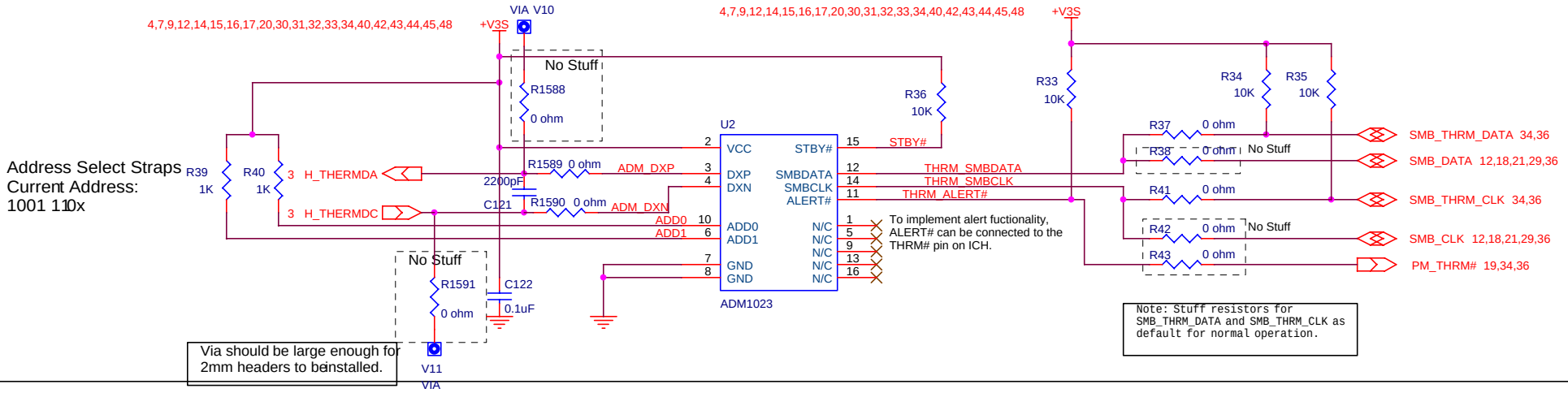


TEST HEADERS

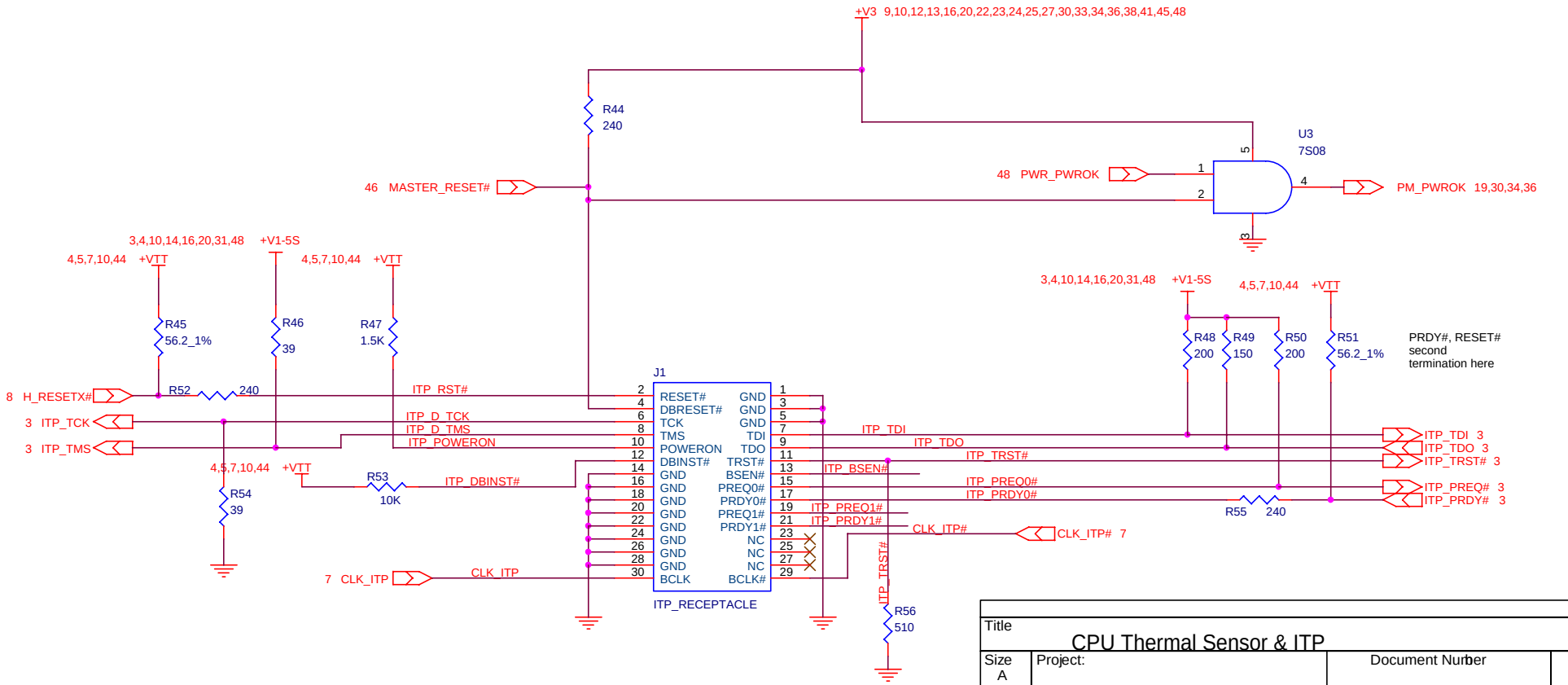
Vias 1-4 should be large enough for 2mm headers to be installed.

Title: CPU Decoupling			
Size: A	Project:	Document Number	Rev
Date:		Sheet 5 of 58	

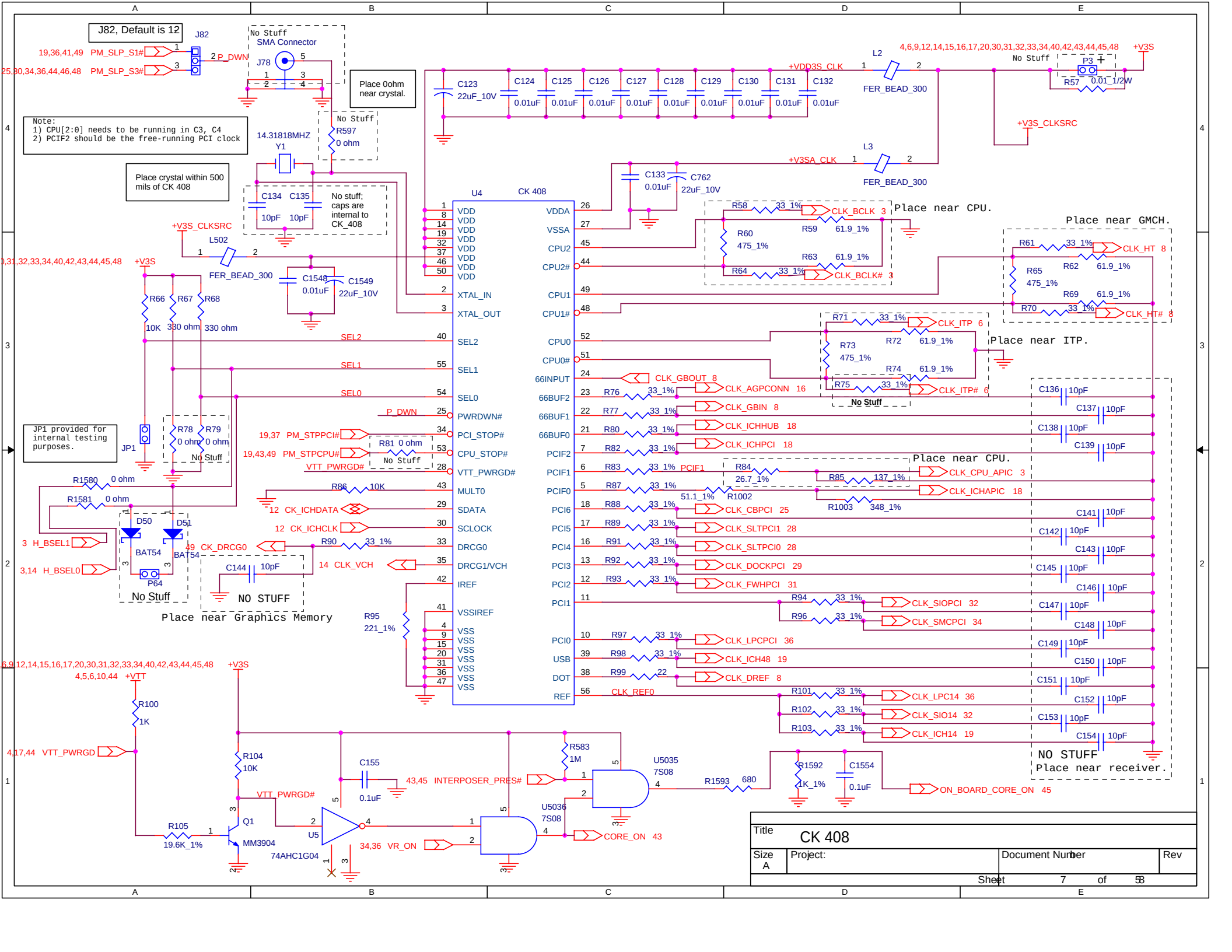
CPU Thermal Sensor



In-Target Probe



Title: CPU Thermal Sensor & ITP			
Size: A	Project:	Document Number	Rev
Date:		Sheet 6 of 58	


J82, Default is 12
J82
19,36,41,49 PM_SLP_S1#
25,30,34,36,44,46,48 PM_SLP_S3#
2 P_DWN
No Stuff
SMA Connector
J78
Place 0ohm near crystal.
Note:
1) CPU[2:0] needs to be running in C3, C4
2) PCIF2 should be the free-running PCI clock
14.31818MHZ
Y1
No Stuff
R597
0 ohm
Place crystal within 500 mils of CK 408
C134 10pF
C135 10pF
No stuff; caps are internal to CK_408
U4
CK 408
C123 22uF_10V
C124 0.01uF
C125 0.01uF
C126 0.01uF
C127 0.01uF
C128 0.01uF
C129 0.01uF
C130 0.01uF
C131 0.01uF
C132 0.01uF
+VDD3S_CLK
L2
FER_BEAD_300
4,6,9,12,14,15,16,17,20,30,31,32,33,34,40,42,43,44,45,48 +V3S
No Stuff
P3
R57 0.01_1/2W
+V3S_CLKSRC
+V3SA_CLK
L3
FER_BEAD_300
C133 0.01uF
C762 22uF_10V
+V3S_CLKSRC
L502
FER_BEAD_300
0,31,32,33,34,40,42,43,44,45,48 +V3S
C1548 0.01uF
C1549 22uF_10V
R66 10K
R67 330 ohm
R68 330 ohm
SEL2
SEL1
SEL0
JP1 provided for internal testing purposes.
JP1
R78 0 ohm
R79 0 ohm
No Stuff
P_DWN
19,37 PM_STPPCI#
19,43,49 PM_STPCPU#
R81 0 ohm
No Stuff
VTT_PWRGD#
R1580 0 ohm
R1581 0 ohm
D50
D51
BAT54
BAT54
3 H_BSEL1
3,14 H_BSEL0
P64
No Stuff
R86 10K
12 CK_ICHDATA
12 CK_ICHCLK
49 CK_DRCG0
R90 33_1%
14 CLK_VCH
C144 10pF
NO STUFF
Place near Graphics Memory
R95 221_1%
XTAL_IN
XTAL_OUT
PWRDWN#
PCI_STOP#
CPU_STOP#
VTT_PWRGD#
MULT0
SDATA
SCLOCK
DRCG0
DRCG1/VCH
IREF
VSSIREF
VDD
VSS
VDDA
VSSA
CPU2
CPU2#
CPU1
CPU1#
CPU0
CPU0#
66INPUT
66BUF2
66BUF1
66BUF0
PCIF2
PCIF1
PCIF0
PCI6
PCI5
PCI4
PCI3
PCI2
PCI1
PCI0
USB
DOT
REF
R58 33_1%
CLK_BCLK 3
R59 61.9_1%
R60 475_1%
R63 61.9_1%
R64 33_1%
CLK_BCLK# 3
Place near CPU.
Place near GMCH.
R61 33_1%
CLK_HT 8
R62 61.9_1%
R65 475_1%
R69 61.9_1%
R70 33_1%
CLK_HT# 8
R71 33_1%
CLK_ITP 6
R72 61.9_1%
R73 475_1%
R74 61.9_1%
R75 33_1%
CLK_ITP# 6
No Stuff
Place near ITP.
CLK_GBOUT 8
R76 33_1%
CLK_AGPCONN 16
R77 33_1%
CLK_GBIN 8
R80 33_1%
CLK_ICHHUB 18
R82 33_1%
CLK_ICHPCI 18
R83 33_1% PCIF1
R84 26.7_1%
R85 137_1%
CLK_CPU_APIC 3
Place near CPU.
R87 33_1%
51.1_1%
R1002
CLK_ICHAPIC 18
R1003 348_1%
R88 33_1%
CLK_CBPCI 25
R89 33_1%
CLK_SLTPCI1 28
R91 33_1%
CLK_SLTPCI0 28
R92 33_1%
CLK_DOCKPCI 29
R93 33_1%
CLK_FWHPCI 31
R94 33_1%
CLK_SIOPCI 32
R96 33_1%
CLK_SMCPCI 34
R97 33_1%
CLK_LPCPCI 36
R98 33_1%
CLK_ICH48 19
R99 22
CLK_DREF 8
CLK_REF0
R101 33_1%
CLK_LPC14 36
R102 33_1%
CLK_SIO14 32
R103 33_1%
CLK_ICH14 19
C136 10pF
C137 10pF
C138 10pF
C139 10pF
C141 10pF
C142 10pF
C143 10pF
C145 10pF
C146 10pF
C147 10pF
C148 10pF
C149 10pF
C150 10pF
C151 10pF
C152 10pF
C153 10pF
C154 10pF
NO STUFF
Place near receiver.
6,9,12,14,15,16,17,20,30,31,32,33,34,40,42,43,44,45,48 +V3S
4,5,6,10,44 +VTT
R100 1K
4,17,44 VTT_PWRGD
R104 10K
R105 19.6K_1%
Q1
MM3904
VTT_PWRGD#
C155 0.1uF
43,45 INTERPOSER_PRES#
R583 1M
U5035 7S08
U5036 7S08
R1593 680
R1592 1K_1%
C1554 0.1uF
ON_BOARD_CORE_ON 45
U5
74AHC1G04
34,36 VR_ON
CORE_ON 43
Title
CK 408
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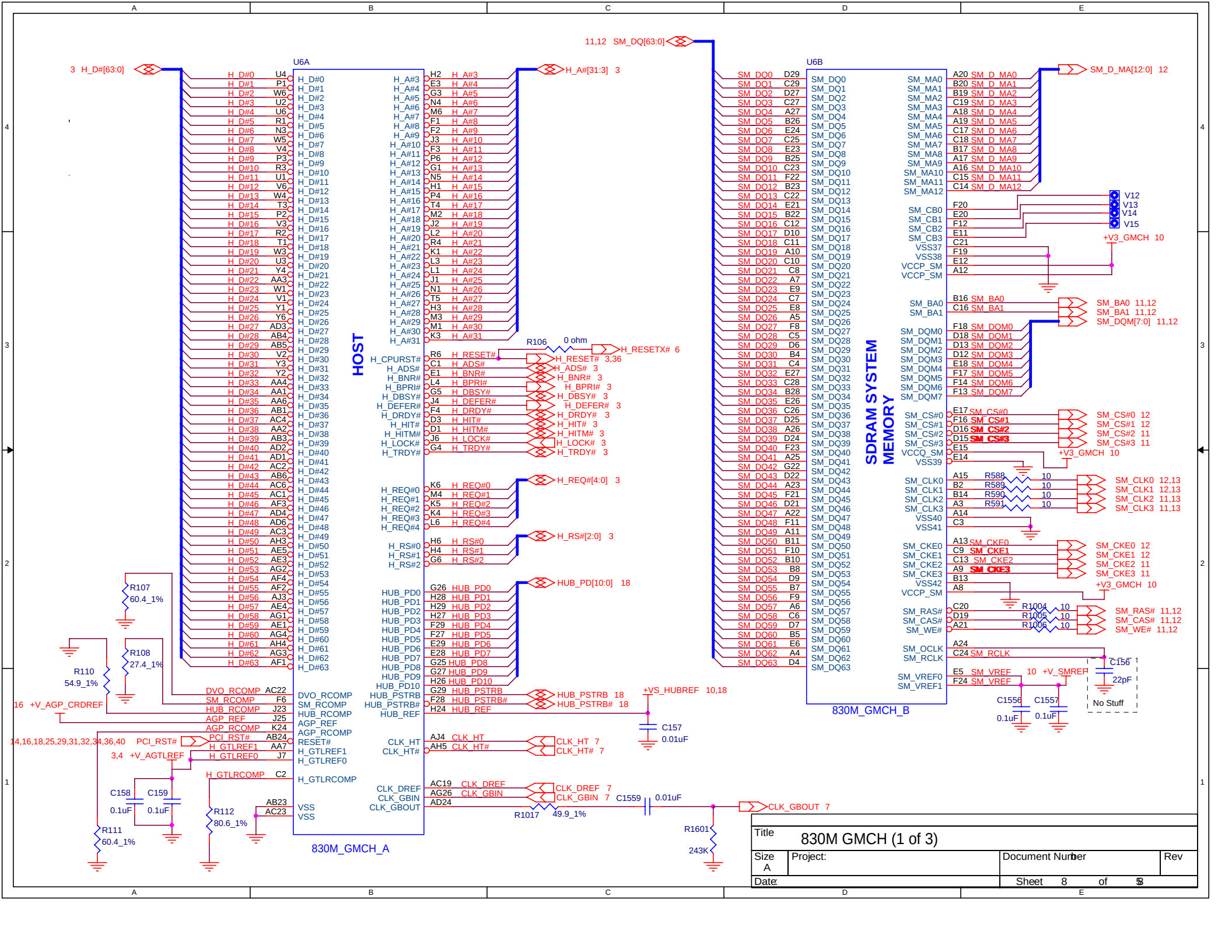
U6A
HOST
830M_GMCH_A
U6B
SDRAM SYSTEM MEMORY
830M_GMCH_B
11,12 SM_DQ[63:0]
3 H_D#[63:0]
H_A#[31:3] 3
SM_D_MA[12:0] 12
R106 0 ohm
H_RESETX# 6
H_REQ#[4:0] 3
H_RS#[2:0] 3
HUB_PD[10:0] 18
+VS_HUBREF 10,18
HUB_PSTRB 18
HUB_PSTRB# 18
CLK_HT 7
CLK_HT# 7
CLK_DREF 7
CLK_GBIN 7
CLK_GBOUT 7
C1559 0.01uF
R1017 49.9_1%
R1601 243K
C157 0.01uF
R107 60.4_1%
R108 27.4_1%
R110 54.9_1%
R111 60.4_1%
R112 80.6_1%
C158 0.1uF
C159 0.1uF
16 +V_AGP_CRDREF
14,16,18,25,29,31,32,34,36,40 PCI_RST#
3,4 +V_AGTLREF
+V3_GMCH 10
+V3_GMCH 10
+V3_GMCH 10
+V_SMREF 10
C156 22pF
No Stuff
C1556 0.1uF
C1557 0.1uF
V12
V13
V14
V15
SM_BA0 11,12
SM_BA1 11,12
SM_DQM[7:0] 11,12
SM_CS#0 12
SM_CS#1 12
SM_CS#2 11
SM_CS#3 11
SM_CLK0 12,13
SM_CLK1 12,13
SM_CLK2 11,13
SM_CLK3 11,13
SM_CKE0 12
SM_CKE1 12
SM_CKE2 11
SM_CKE3 11
SM_RAS# 11,12
SM_CAS# 11,12
SM_WE# 11,12
Title 830M GMCH (1 of 3)
Size A
Project:
Document Number
Rev
Date:
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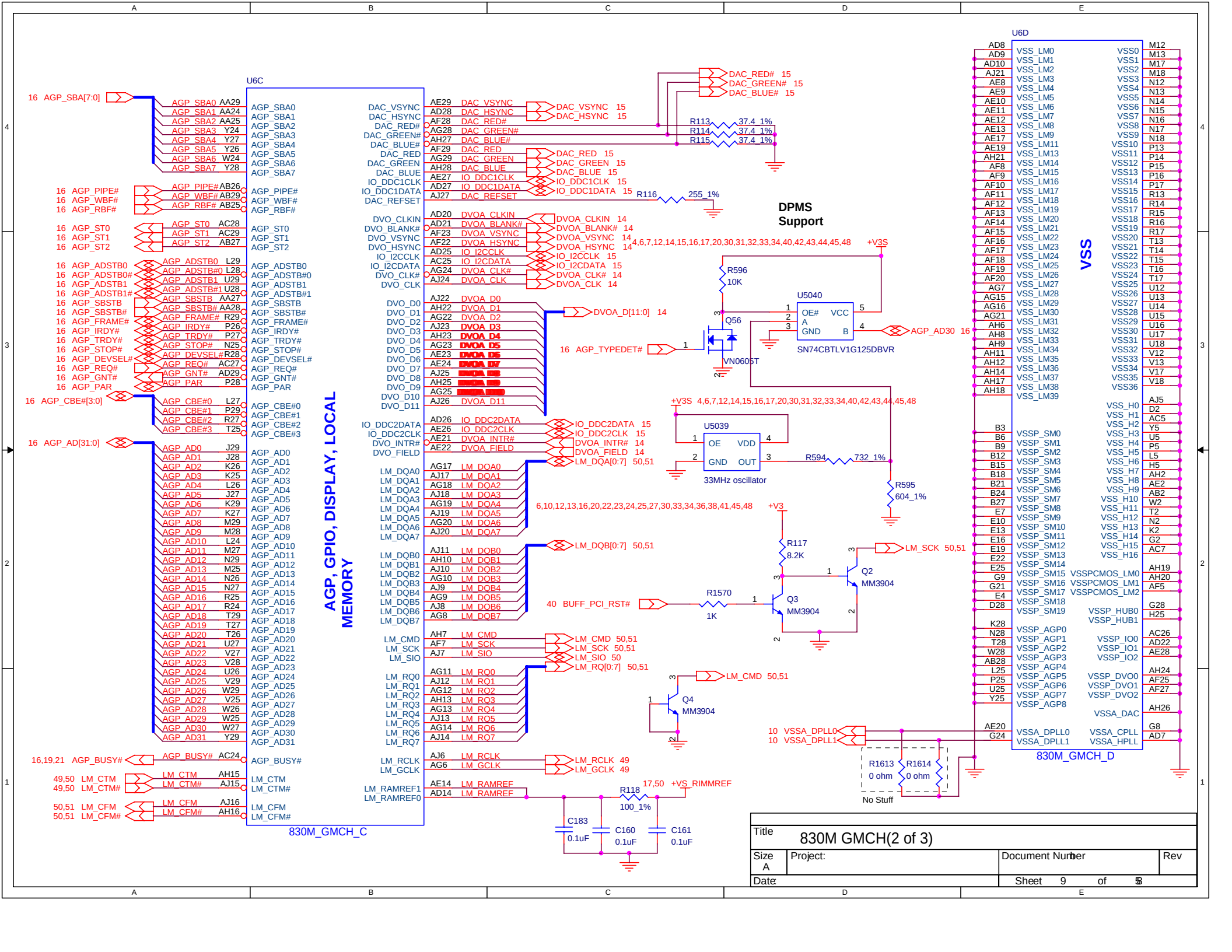
U6C
AGP, GPIO, DISPLAY, LOCAL MEMORY
830M_GMCH_C
DPMS Support
U5040
SN74CBTLV1G125DBVR
U5039
33MHz oscillator
U6D
VSS
830M_GMCH_D
No Stuff
Title
830M GMCH(2 of 3)
Size A
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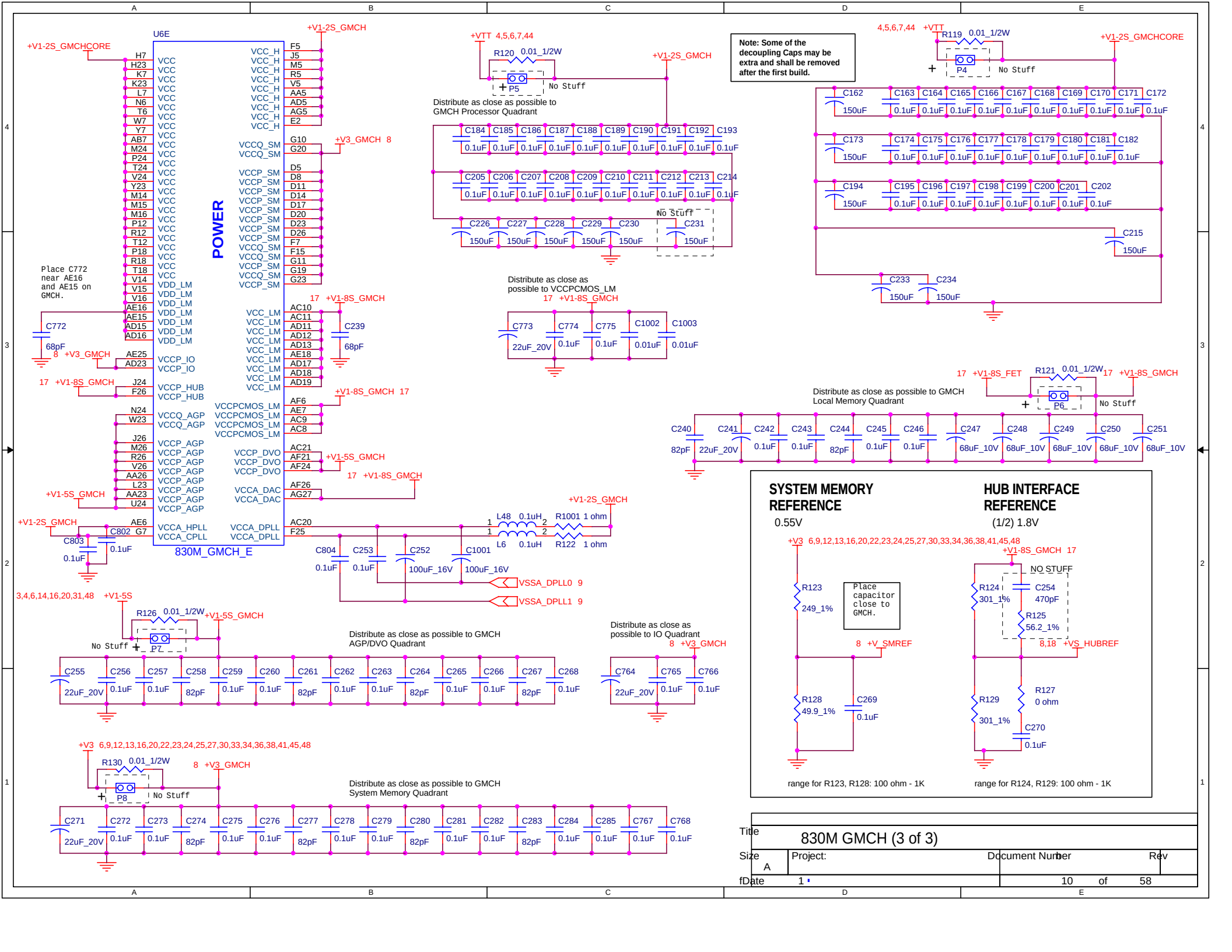
U6E
POWER
830M_GMCH_E
+V1-2S_GMCHCORE
+V1-2S_GMCH
+V3_GMCH 8
+V1-8S_GMCH 17
+V1-5S_GMCH 17
+V1-5S_GMCH
+V1-5S
+V1-8S_GMCH
+V1-8S_FET
+V1-2S_GMCH
+VTT 4,5,6,7,44
+V3 6,9,12,13,16,20,22,23,24,25,27,30,33,34,36,38,41,45,48
3,4,6,14,16,20,31,48 +V1-5S
8 +V3_GMCH
8 +V_SMREF
8,18 +VS_HUBREF
17 +V1-8S_GMCH
17 +V1-8S_FET
4,5,6,7,44 +VTT
VSSA_DPLL0 9
VSSA_DPLL1 9
Note: Some of the decoupling Caps may be extra and shall be removed after the first build.
Place C772 near AE16 and AE15 on GMCH.
Distribute as close as possible to GMCH Processor Quadrant
Distribute as close as possible to VCCPCMOS_LM
Distribute as close as possible to GMCH Local Memory Quadrant
Distribute as close as possible to GMCH AGP/DVO Quadrant
Distribute as close as possible to IO Quadrant
Distribute as close as possible to GMCH System Memory Quadrant
Place capacitor close to GMCH.
No Stuff
SYSTEM MEMORY REFERENCE
0.55V
HUB INTERFACE REFERENCE
(1/2) 1.8V
range for R123, R128: 100 ohm - 1K
range for R124, R129: 100 ohm - 1K
Title
830M GMCH (3 of 3)
Size
A
Project:
Document Number
Rev
fDate
1
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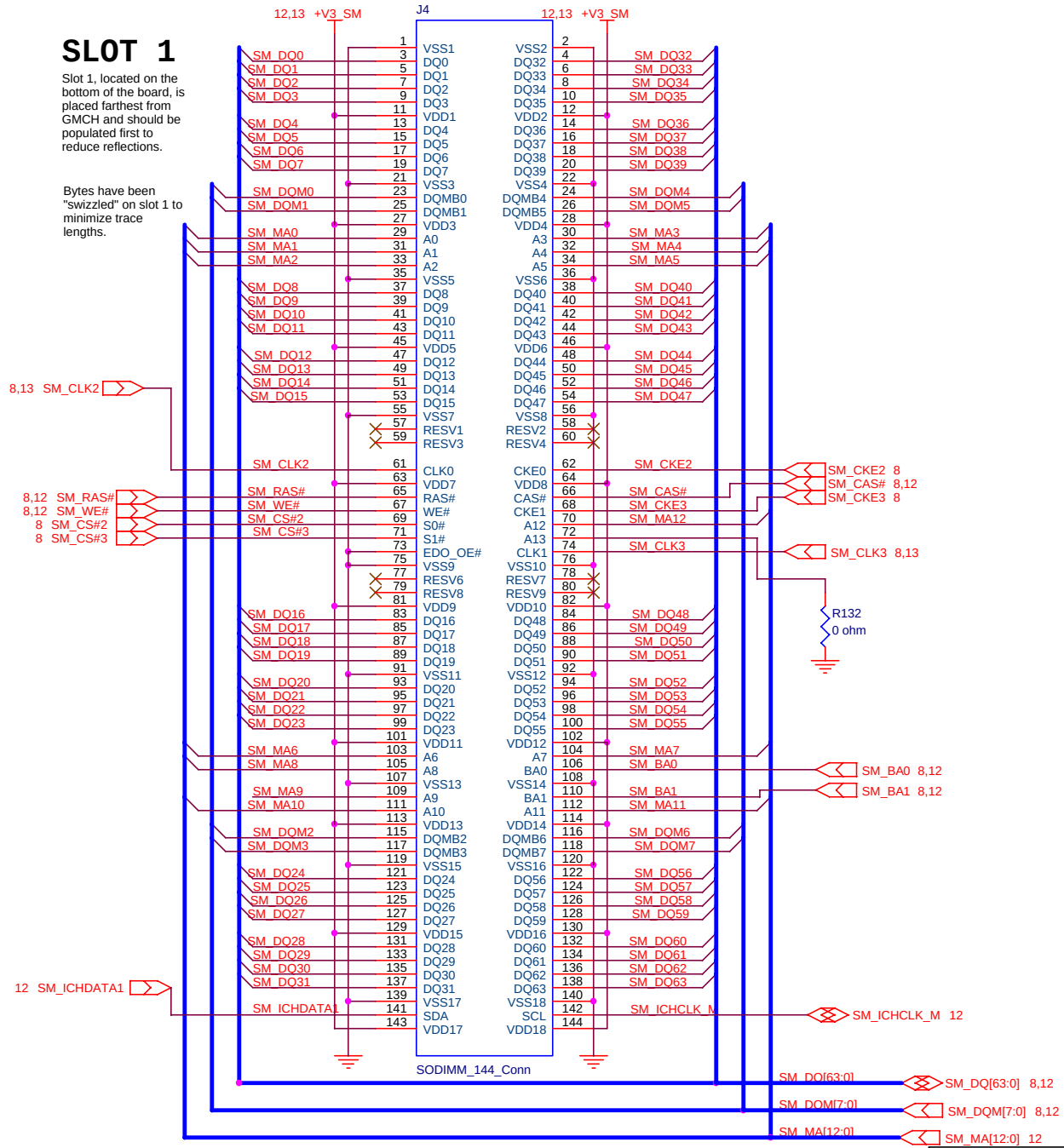
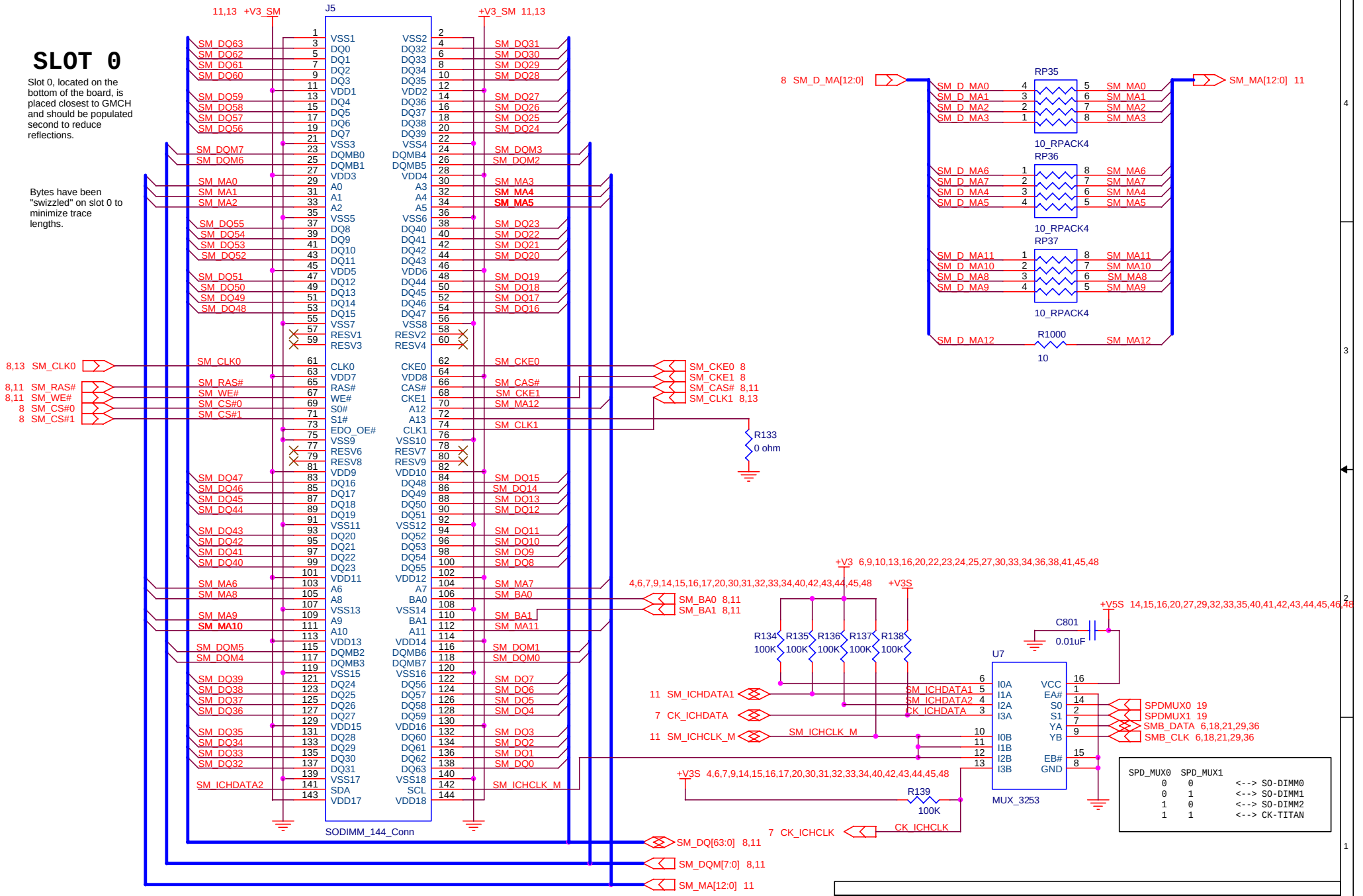


Title	SDRAM SO-DIMM 1 of 2		
Size A	Project:	Document Number	Rev
Date: 1		Sheet 11 of 58	

SLOT 0

Slot 0, located on the bottom of the board, is placed closest to GMCH and should be populated second to reduce reflections.

Bytes have been "swizzled" on slot 0 to minimize trace lengths.



Title	SDRAM SO-DIMM 2 of 2		
Size A	Project:	Document Number	Rev
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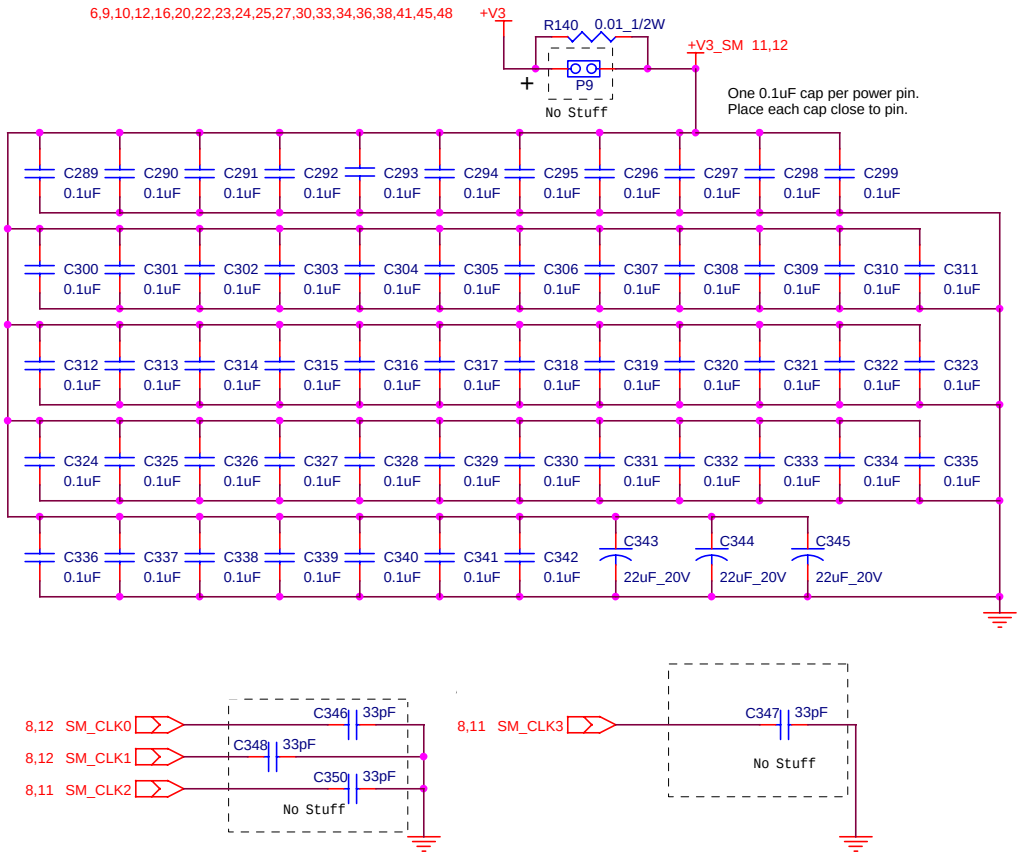

Title: SDRAM Decoupling			
Size: A	Project:	Document Number	Rev
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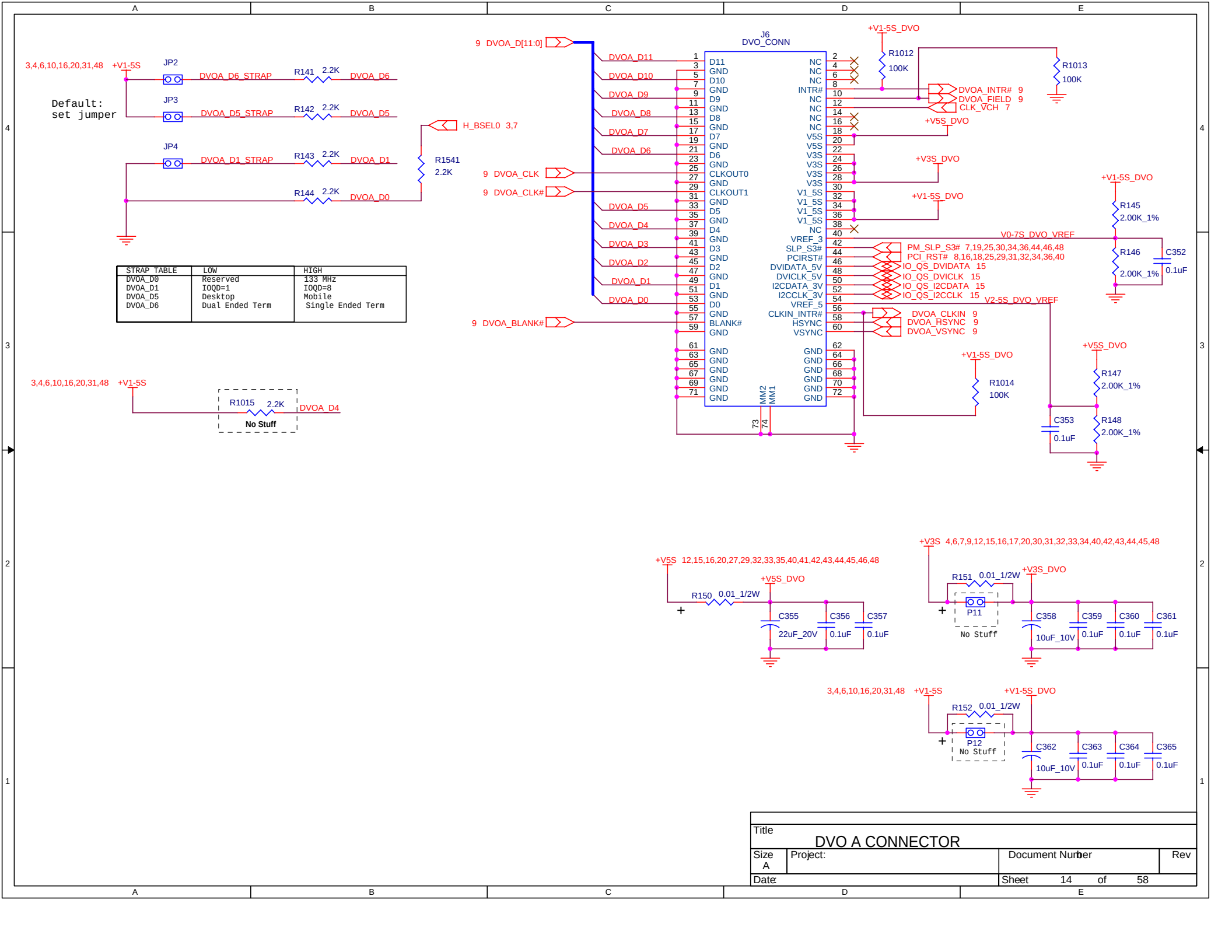
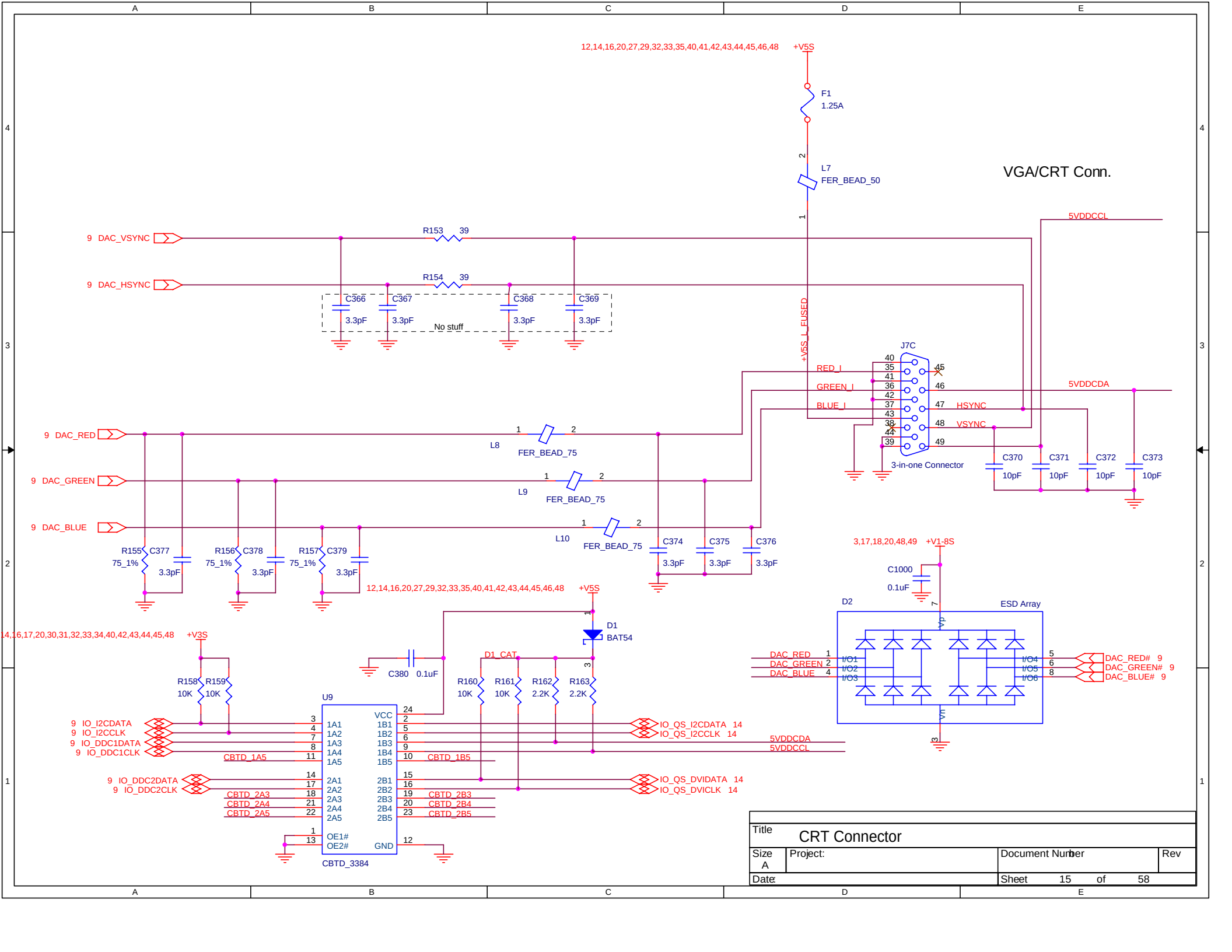

3,4,6,10,16,20,31,48 +V1-5S
JP2
DVOA_D6_STRAP
R141 2.2K
DVOA_D6
Default:
set jumper
JP3
DVOA_D5_STRAP
R142 2.2K
DVOA_D5
JP4
DVOA_D1_STRAP
R143 2.2K
DVOA_D1
R144 2.2K
DVOA_D0
H_BSEL0 3,7
R1541
2.2K
STRAP TABLE | LOW | HIGH
DVOA_D0 | Reserved | 133 MHz
DVOA_D1 | IOQD=1 | IOQD=8
DVOA_D5 | Desktop | Mobile
DVOA_D6 | Dual Ended Term | Single Ended Term
3,4,6,10,16,20,31,48 +V1-5S
R1015 2.2K
No Stuff
DVOA_D4
9 DVOA_D[11:0]
9 DVOA_CLK
9 DVOA_CLK#
9 DVOA_BLANK#
J6
DVO_CONN
DVOA_D11
DVOA_D10
DVOA_D9
DVOA_D8
DVOA_D7
DVOA_D6
DVOA_D5
DVOA_D4
DVOA_D3
DVOA_D2
DVOA_D1
DVOA_D0
D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 BLANK#
CLKOUT0 CLKOUT1
GND
NC
INTR#
V5S
V3S
V1_5S
VREF_3
SLP_S3#
PCIRST#
DVIDATA_5V
DVICLK_5V
I2CDATA_3V
I2CCLK_3V
VREF_5
CLKIN_INTR#
HSYNC
VSYNC
MM2
MM1
+V1-5S_DVO
R1012 100K
R1013 100K
DVOA_INTR# 9
DVOA_FIELD 9
CLK_VCH 7
+V5S_DVO
+V3S_DVO
+V1-5S_DVO
V0-7S_DVO_VREF
R145 2.00K_1%
R146 2.00K_1%
C352 0.1uF
PM_SLP_S3# 7,19,25,30,34,36,44,46,48
PCI_RST# 8,16,18,25,29,31,32,34,36,40
IO_QS_DVIDATA 15
IO_QS_DVICLK 15
IO_QS_I2CDATA 15
IO_QS_I2CCLK 15
V2-5S_DVO_VREF
DVOA_CLKIN 9
DVOA_HSYNC 9
DVOA_VSYNC 9
+V1-5S_DVO
R1014 100K
+V5S_DVO
R147 2.00K_1%
R148 2.00K_1%
C353 0.1uF
+V5S 12,15,16,20,27,29,32,33,35,40,41,42,43,44,45,46,48
+V5S_DVO
R150 0.01_1/2W
C355 22uF_20V
C356 0.1uF
C357 0.1uF
+V3S 4,6,7,9,12,15,16,17,20,30,31,32,33,34,40,42,43,44,45,48
+V3S_DVO
R151 0.01_1/2W
P11
No Stuff
C358 10uF_10V
C359 0.1uF
C360 0.1uF
C361 0.1uF
3,4,6,10,16,20,31,48 +V1-5S
+V1-5S_DVO
R152 0.01_1/2W
P12
No Stuff
C362 10uF_10V
C363 0.1uF
C364 0.1uF
C365 0.1uF
Title
DVO A CONNECTOR
Size A
Project:
Document Number
Rev
Date:
Sheet 14 of 58


VGA/CRT Conn.
12,14,16,20,27,29,32,33,35,40,41,42,43,44,45,46,48 +V5S
F1
1.25A
L7
FER_BEAD_50
+V5S_L_FUSED
5VDDCCL
5VDDCDA
9 DAC_VSYNC
9 DAC_HSYNC
R153 39
R154 39
C366 3.3pF
C367 3.3pF
C368 3.3pF
C369 3.3pF
No stuff
J7C
3-in-one Connector
RED_I
GREEN_I
BLUE_I
HSYNC
VSYNC
C370 10pF
C371 10pF
C372 10pF
C373 10pF
9 DAC_RED
9 DAC_GREEN
9 DAC_BLUE
L8 FER_BEAD_75
L9 FER_BEAD_75
L10 FER_BEAD_75
R155 75_1% C377 3.3pF
R156 75_1% C378 3.3pF
R157 75_1% C379 3.3pF
C374 3.3pF
C375 3.3pF
C376 3.3pF
3,17,18,20,48,49 +V1-8S
C1000 0.1uF
D2
ESD Array
DAC_RED
DAC_GREEN
DAC_BLUE
DAC_RED# 9
DAC_GREEN# 9
DAC_BLUE# 9
12,14,16,20,27,29,32,33,35,40,41,42,43,44,45,46,48 +V5S
D1
BAT54
D1_CAT
C380 0.1uF
4,16,17,20,30,31,32,33,34,40,42,43,44,45,48 +V3S
R158 10K
R159 10K
R160 10K
R161 10K
R162 2.2K
R163 2.2K
U9
9 IO_I2CDATA
9 IO_I2CCLK
9 IO_DDC1DATA
9 IO_DDC1CLK
CBTD_1A5
CBTD_1B5
IO_QS_I2CDATA 14
IO_QS_I2CCLK 14
5VDDCDA
5VDDCCL
9 IO_DDC2DATA
9 IO_DDC2CLK
CBTD_2A3
CBTD_2A4
CBTD_2A5
CBTD_2B3
CBTD_2B4
CBTD_2B5
IO_QS_DVIDATA 14
IO_QS_DVICLK 14
CBTD_3384
Title CRT Connector
Size A
Project:
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Rev
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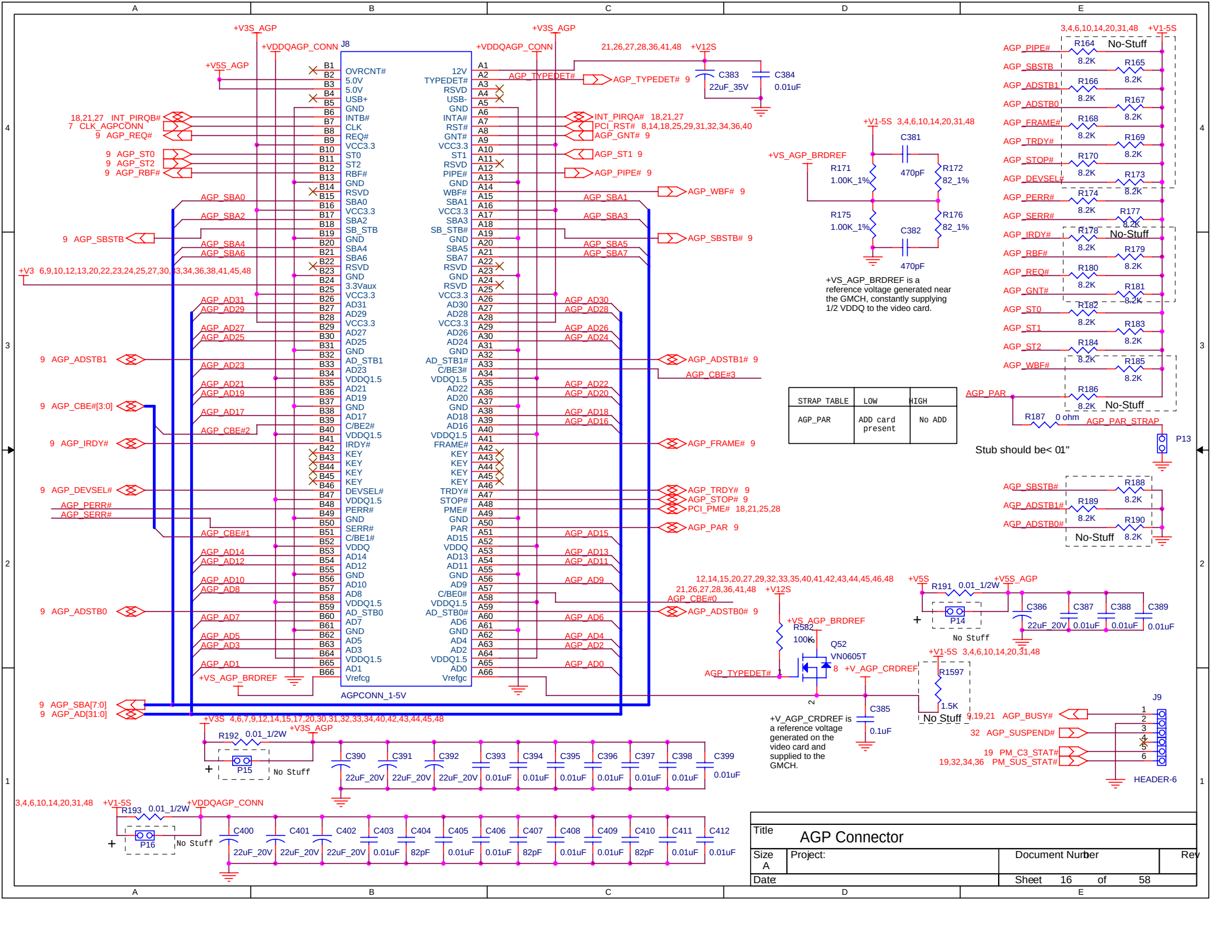
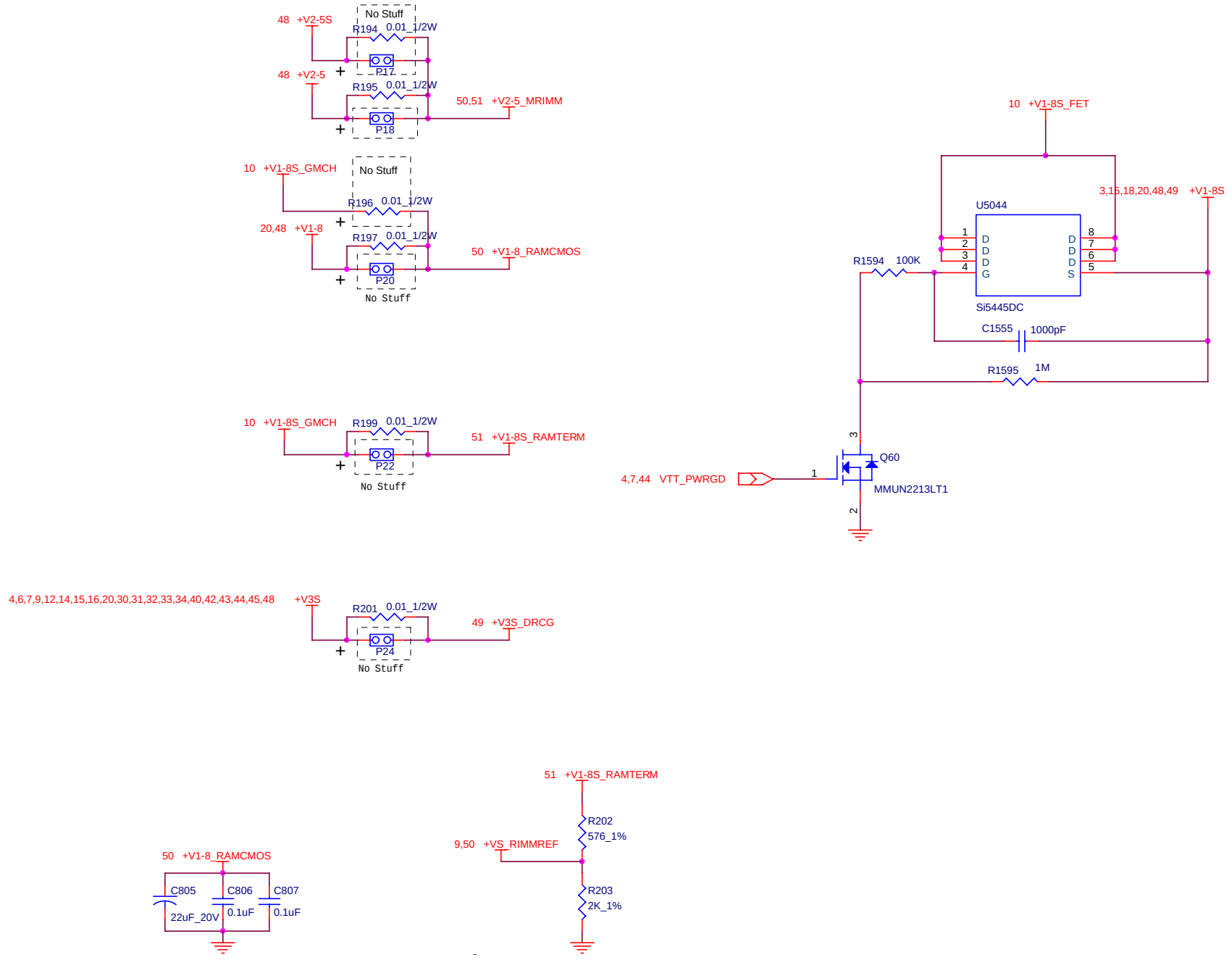
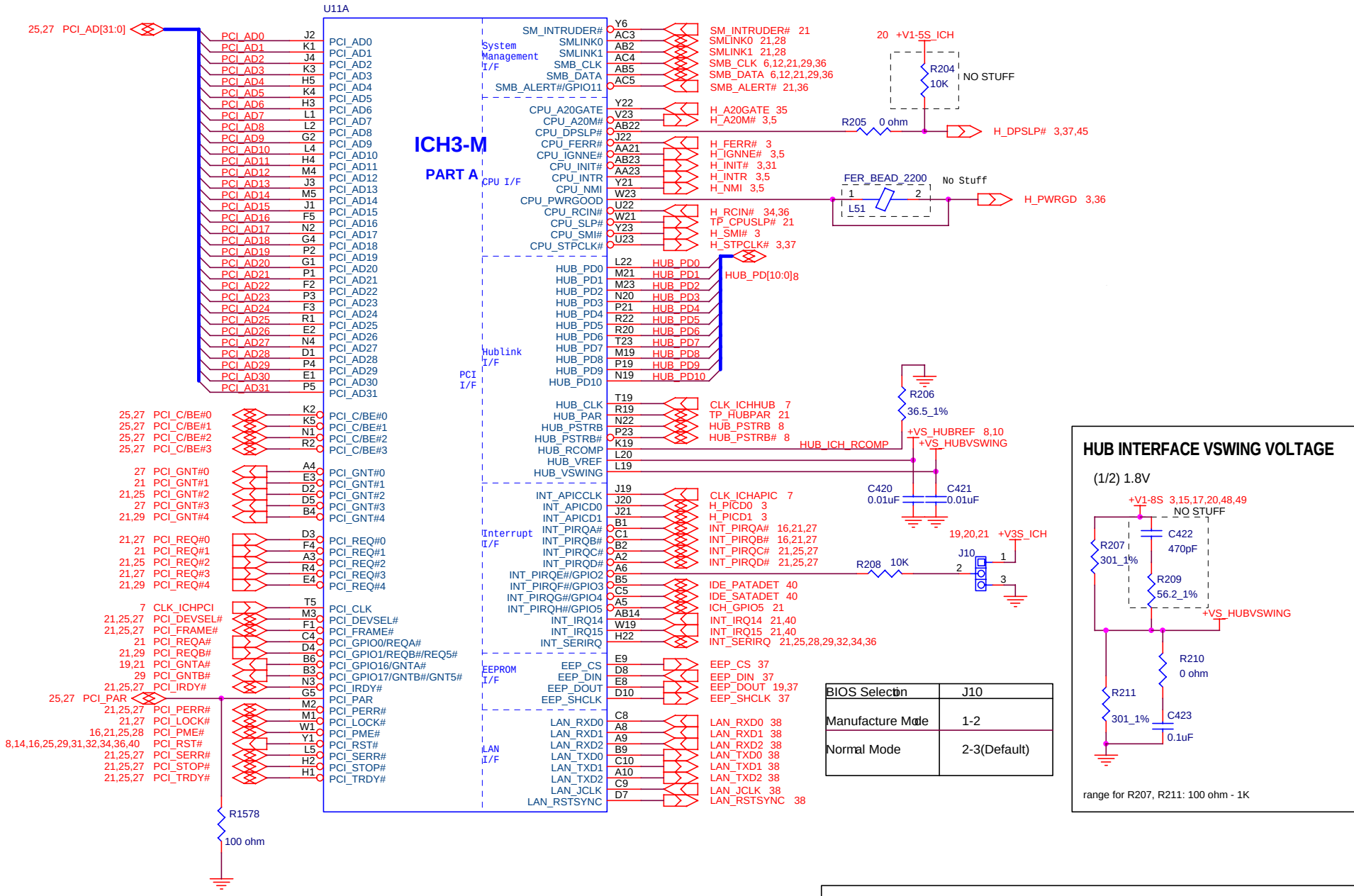

J8
AGPCONN_1-5V
+V3S_AGP
+VDDQAGP_CONN
+V5S_AGP
+V12S
+V1-5S
+VS_AGP_BRDREF
+V_AGP_CRDREF
AGP_TYPEDET#
AGP_PAR
AGP_PAR_STRAP
AGP_BUSY#
AGP_SUSPEND#
PM_C3_STAT#
PM_SUS_STAT#
HEADER-6
No Stuff
No-Stuff
Stub should be< 01"
+VS_AGP_BRDREF is a reference voltage generated near the GMCH, constantly supplying 1/2 VDDQ to the video card.
+V_AGP_CRDREF is a reference voltage generated on the video card and supplied to the GMCH.
STRAP TABLE | LOW | HIGH
AGP_PAR | ADD card present | No ADD
Title
AGP Connector
Size A
Project:
Document Number
Rev
Date
Sheet 16 of 58



Title	Graphics Local Memory Power Measurement		
Size A	Project:	Document Number	Rev
Date:		Sheet 17 of 58	


U11A
ICH3-M
PART A
25,27 PCI_AD[31:0]
PCI_AD0 J2
PCI_AD1 K1
PCI_AD2 J4
PCI_AD3 K3
PCI_AD4 H5
PCI_AD5 K4
PCI_AD6 H3
PCI_AD7 L1
PCI_AD8 L2
PCI_AD9 G2
PCI_AD10 L4
PCI_AD11 H4
PCI_AD12 M4
PCI_AD13 J3
PCI_AD14 M5
PCI_AD15 J1
PCI_AD16 F5
PCI_AD17 N2
PCI_AD18 G4
PCI_AD19 P2
PCI_AD20 G1
PCI_AD21 P1
PCI_AD22 F2
PCI_AD23 P3
PCI_AD24 F3
PCI_AD25 R1
PCI_AD26 E2
PCI_AD27 N4
PCI_AD28 D1
PCI_AD29 P4
PCI_AD30 E1
PCI_AD31 P5
25,27 PCI_C/BE#0 K2
25,27 PCI_C/BE#1 K5
25,27 PCI_C/BE#2 N1
25,27 PCI_C/BE#3 R2
27 PCI_GNT#0 A4
21 PCI_GNT#1 E3
21,25 PCI_GNT#2 D2
27 PCI_GNT#3 D5
21,29 PCI_GNT#4 B4
21,27 PCI_REQ#0 D3
21 PCI_REQ#1 F4
21,25 PCI_REQ#2 A3
21,27 PCI_REQ#3 R4
21,29 PCI_REQ#4 E4
7 CLK_ICHPCI T5
21,25,27 PCI_DEVSEL# M3
21,25,27 PCI_FRAME# F1
21 PCI_REQA# C4
21,29 PCI_REQB# D4
19,21 PCI_GNTA# B6
29 PCI_GNTB# B3
21,25,27 PCI_IRDY# N3
25,27 PCI_PAR G5
21,25,27 PCI_PERR# M2
21,27 PCI_LOCK# M1
16,21,25,28 PCI_PME# W1
8,14,16,25,29,31,32,34,36,40 PCI_RST# Y1
21,25,27 PCI_SERR# L5
21,25,27 PCI_STOP# H2
21,25,27 PCI_TRDY# H1
R1578
100 ohm
System Management I/F
SM_INTRUDER# Y6
SMLINK0 AC3
SMLINK1 AB2
SMB_CLK AC4
SMB_DATA AB5
SMB_ALERT#/GPIO11 AC5
SM_INTRUDER# 21
SMLINK0 21,28
SMLINK1 21,28
SMB_CLK 6,12,21,29,36
SMB_DATA 6,12,21,29,36
SMB_ALERT# 21,36
CPU I/F
CPU_A20GATE Y22
CPU_A20M# V23
CPU_DPSLP# AB22
CPU_FERR# J22
CPU_IGNNE# AA21
CPU_INIT# AB23
CPU_INTR AA23
CPU_NMI Y21
CPU_PWRGOOD W23
CPU_RCIN# U22
CPU_SLP# W21
CPU_SMI# Y23
CPU_STPCLK# U23
H_A20GATE 35
H_A20M# 3,5
H_FERR# 3
H_IGNNE# 3,5
H_INIT# 3,31
H_INTR 3,5
H_NMI 3,5
H_RCIN# 34,36
TP_CPUSLP# 21
H_SMI# 3
H_STPCLK# 3,37
20 +V1-5S_ICH
R204
10K
NO STUFF
R205 0 ohm
H_DPSLP# 3,37,45
FER_BEAD_2200
No Stuff
L51
H_PWRGD 3,36
Hublink I/F
HUB_PD0 L22
HUB_PD1 M21
HUB_PD2 M23
HUB_PD3 N20
HUB_PD4 P21
HUB_PD5 R22
HUB_PD6 R20
HUB_PD7 T23
HUB_PD8 M19
HUB_PD9 P19
HUB_PD10 N19
HUB_PD[10:0]8
PCI I/F
HUB_CLK T19
HUB_PAR R19
HUB_PSTRB N22
HUB_PSTRB# P23
HUB_RCOMP K19
HUB_VREF L20
HUB_VSWING L19
CLK_ICHHUB 7
TP_HUBPAR 21
HUB_PSTRB 8
HUB_PSTRB# 8
R206
36.5_1%
+VS_HUBREF 8,10
+VS_HUBVSWING
HUB_ICH_RCOMP
C420
0.01uF
C421
0.01uF
Interrupt I/F
INT_APICCLK J19
INT_APICD0 J20
INT_APICD1 J21
INT_PIRQA# B1
INT_PIRQB# C1
INT_PIRQC# B2
INT_PIRQD# A2
INT_PIRQE#/GPIO2 A6
INT_PIRQF#/GPIO3 B5
INT_PIRQG#/GPIO4 C5
INT_PIRQH#/GPIO5 A5
INT_IRQ14 AB14
INT_IRQ15 W19
INT_SERIRQ H22
CLK_ICHAPIC 7
H_PICD0 3
H_PICD1 3
INT_PIRQA# 16,21,27
INT_PIRQB# 16,21,27
INT_PIRQC# 21,25,27
INT_PIRQD# 21,25,27
19,20,21 +V3S_ICH
J10
R208 10K
IDE_PATADET 40
IDE_SATADET 40
ICH_GPIO5 21
INT_IRQ14 21,40
INT_IRQ15 21,40
INT_SERIRQ 21,25,28,29,32,34,36
EEPROM I/F
EEP_CS E9
EEP_DIN D8
EEP_DOUT E8
EEP_SHCLK D10
EEP_CS 37
EEP_DIN 37
EEP_DOUT 19,37
EEP_SHCLK 37
LAN I/F
LAN_RXD0 C8
LAN_RXD1 A8
LAN_RXD2 A9
LAN_TXD0 B9
LAN_TXD1 C10
LAN_TXD2 A10
LAN_JCLK C9
LAN_RSTSYNC D7
LAN_RXD0 38
LAN_RXD1 38
LAN_RXD2 38
LAN_TXD0 38
LAN_TXD1 38
LAN_TXD2 38
LAN_JCLK 38
LAN_RSTSYNC 38
BIOS Selection J10
Manufacture Mode 1-2
Normal Mode 2-3(Default)
HUB INTERFACE VSWING VOLTAGE
(1/2) 1.8V
+V1-8S 3,15,17,20,48,49
NO STUFF
C422
470pF
R207
301_1%
R209
56.2_1%
+VS_HUBVSWING
R210
0 ohm
R211
301_1%
C423
0.1uF
range for R207, R211: 100 ohm - 1K
Title
ICH3-M (1 of 3)
Size A
Project:
Document Number
Rev
Date:
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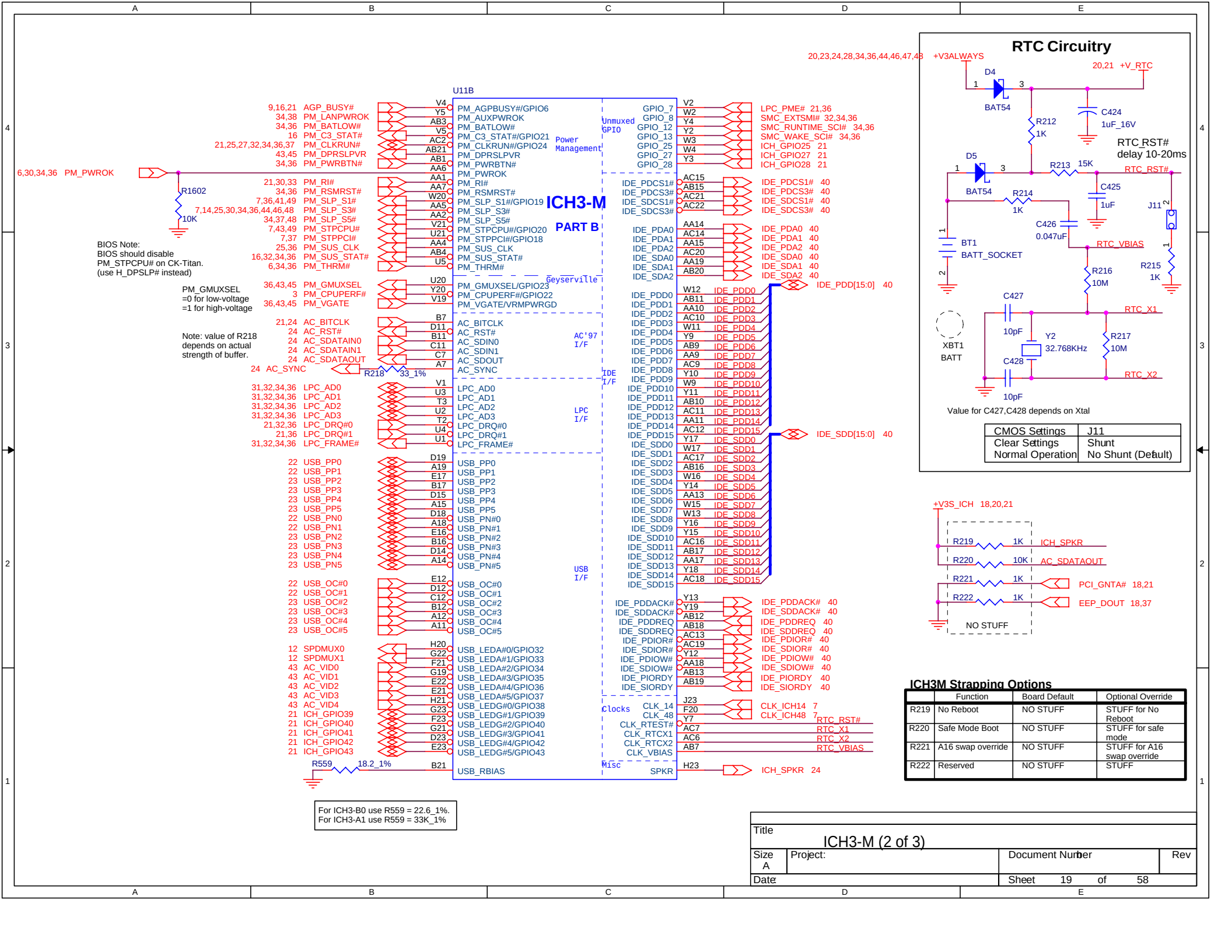

ICH3M Strapping Options

	Function	Board Default	Optional Override
R219	No Reboot	NO STUFF	STUFF for No Reboot
R220	Safe Mode Boot	NO STUFF	STUFF for safe mode
R221	A16 swap override	NO STUFF	STUFF for A16 swap override
R222	Reserved	NO STUFF	STUFF

Title: ICH3-M (2 of 3)			
Size: A	Project:	Document Number	Rev
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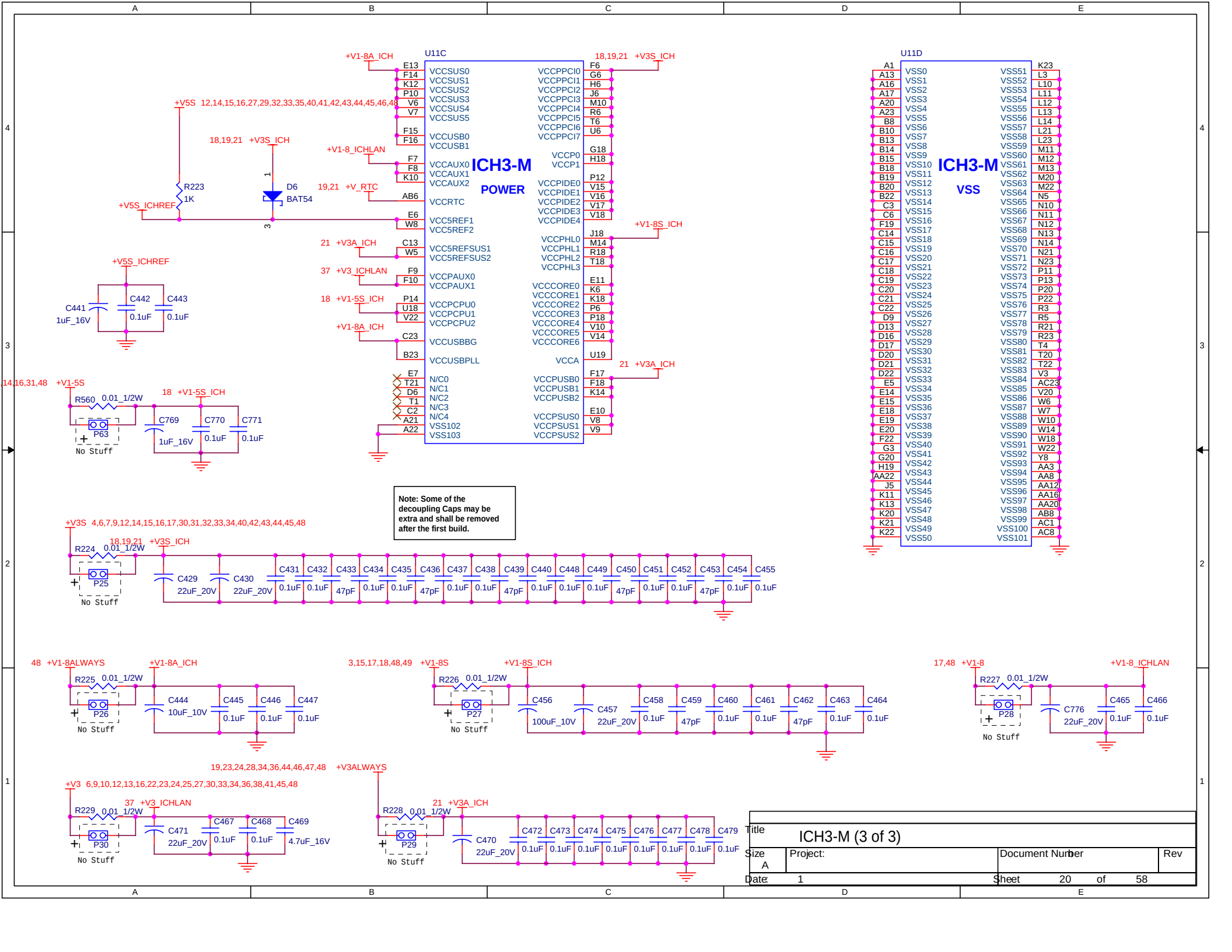
U11C
ICH3-M
POWER
U11D
ICH3-M
VSS
Note: Some of the decoupling Caps may be extra and shall be removed after the first build.
Title
ICH3-M (3 of 3)
Size
A
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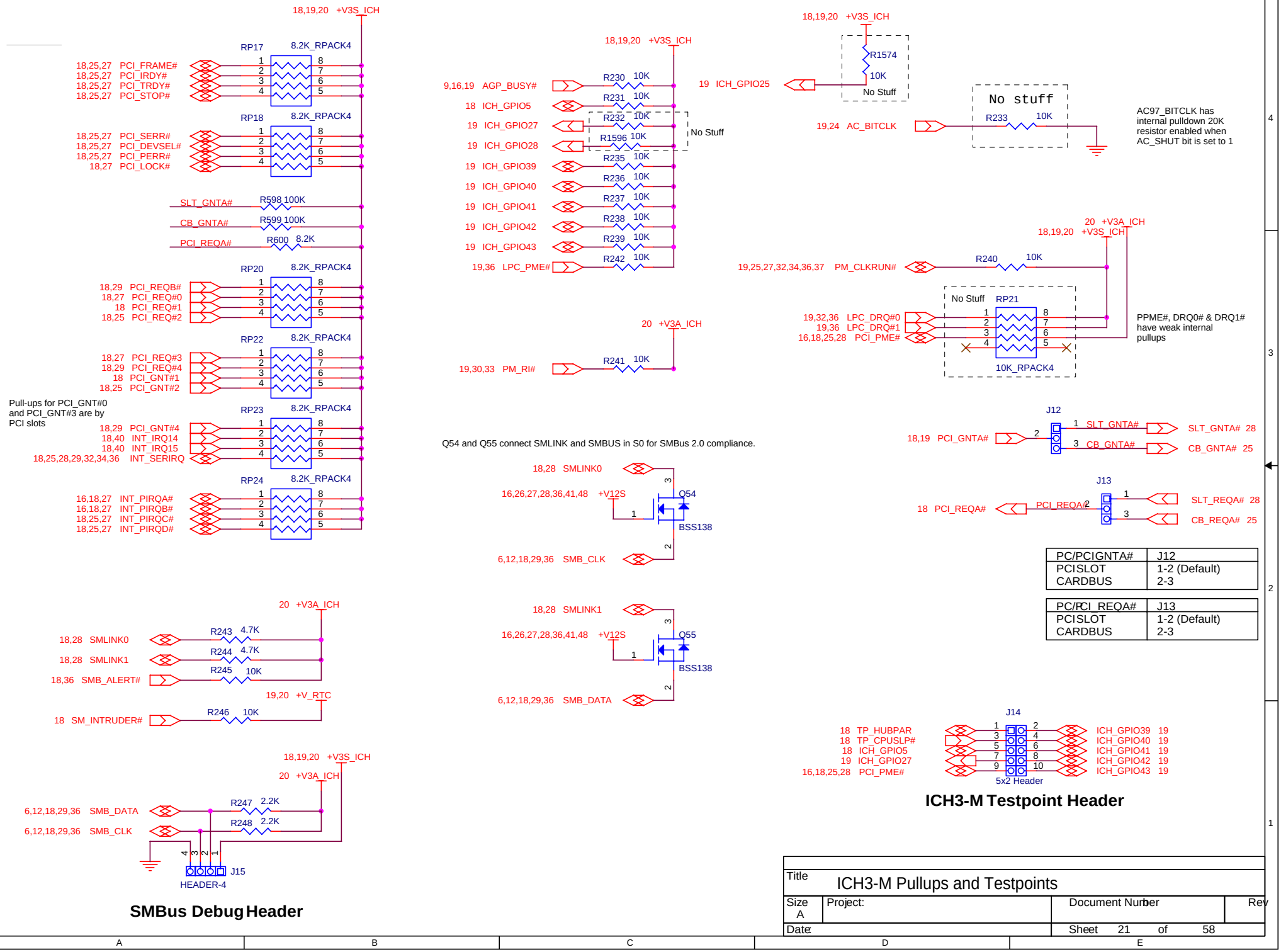
Sheet
20
of
58


18,19,20 +V3S_ICH
RP17 8.2K_RPACK4
18,25,27 PCI_FRAME#
18,25,27 PCI_IRDY#
18,25,27 PCI_TRDY#
18,25,27 PCI_STOP#
RP18 8.2K_RPACK4
18,25,27 PCI_SERR#
18,25,27 PCI_DEVSEL#
18,25,27 PCI_PERR#
18,27 PCI_LOCK#
SLT_GNTA# R598 100K
CB_GNTA# R599 100K
PCI_REQA# R600 8.2K
RP20 8.2K_RPACK4
18,29 PCI_REQB#
18,27 PCI_REQ#0
18 PCI_REQ#1
18,25 PCI_REQ#2
RP22 8.2K_RPACK4
18,27 PCI_REQ#3
18,29 PCI_REQ#4
18 PCI_GNT#1
18,25 PCI_GNT#2
Pull-ups for PCI_GNT#0 and PCI_GNT#3 are by PCI slots
RP23 8.2K_RPACK4
18,29 PCI_GNT#4
18,40 INT_IRQ14
18,40 INT_IRQ15
18,25,28,29,32,34,36 INT_SERIRQ
RP24 8.2K_RPACK4
16,18,27 INT_PIRQA#
16,18,27 INT_PIRQB#
18,25,27 INT_PIRQC#
18,25,27 INT_PIRQD#
20 +V3A_ICH
18,28 SMLINK0 R243 4.7K
18,28 SMLINK1 R244 4.7K
18,36 SMB_ALERT# R245 10K
19,20 +V_RTC
18 SM_INTRUDER# R246 10K
18,19,20 +V3S_ICH
20 +V3A_ICH
6,12,18,29,36 SMB_DATA R247 2.2K
6,12,18,29,36 SMB_CLK R248 2.2K
J15
HEADER-4
SMBus Debug Header
18,19,20 +V3S_ICH
9,16,19 AGP_BUSY# R230 10K
18 ICH_GPIO5 R231 10K
19 ICH_GPIO27 R232 10K
19 ICH_GPIO28 R1596 10K
No Stuff
19 ICH_GPIO39 R235 10K
19 ICH_GPIO40 R236 10K
19 ICH_GPIO41 R237 10K
19 ICH_GPIO42 R238 10K
19 ICH_GPIO43 R239 10K
19,36 LPC_PME# R242 10K
20 +V3A_ICH
19,30,33 PM_RI# R241 10K
Q54 and Q55 connect SMLINK and SMBUS in S0 for SMBus 2.0 compliance.
18,28 SMLINK0
16,26,27,28,36,41,48 +V12S
Q54
BSS138
6,12,18,29,36 SMB_CLK
18,28 SMLINK1
16,26,27,28,36,41,48 +V12S
Q55
BSS138
6,12,18,29,36 SMB_DATA
18,19,20 +V3S_ICH
19 ICH_GPIO25 R1574 10K
No Stuff
19,24 AC_BITCLK
No stuff R233 10K
AC97_BITCLK has internal pulldown 20K resistor enabled when AC_SHUT bit is set to 1
20 +V3A_ICH
18,19,20 +V3S_ICH
19,25,27,32,34,36,37 PM_CLKRUN# R240 10K
No Stuff RP21
19,32,36 LPC_DRQ#0
19,36 LPC_DRQ#1
16,18,25,28 PCI_PME#
10K_RPACK4
PPME#, DRQ0# & DRQ1# have weak internal pullups
J12
18,19 PCI_GNTA#
SLT_GNTA#
CB_GNTA#
SLT_GNTA# 28
CB_GNTA# 25
J13
18 PCI_REQA#
PCI_REQA#
SLT_REQA# 28
CB_REQA# 25
PC/PCIGNTA# J12
PCISLOT 1-2 (Default)
CARDBUS 2-3
PC/PCI_REQA# J13
PCISLOT 1-2 (Default)
CARDBUS 2-3
J14
18 TP_HUBPAR
18 TP_CPUSLP#
18 ICH_GPIO5
19 ICH_GPIO27
16,18,25,28 PCI_PME#
ICH_GPIO39 19
ICH_GPIO40 19
ICH_GPIO41 19
ICH_GPIO42 19
ICH_GPIO43 19
5x2 Header
ICH3-M Testpoint Header
Title ICH3-M Pullups and Testpoints
Size A
Project:
Document Number
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Date
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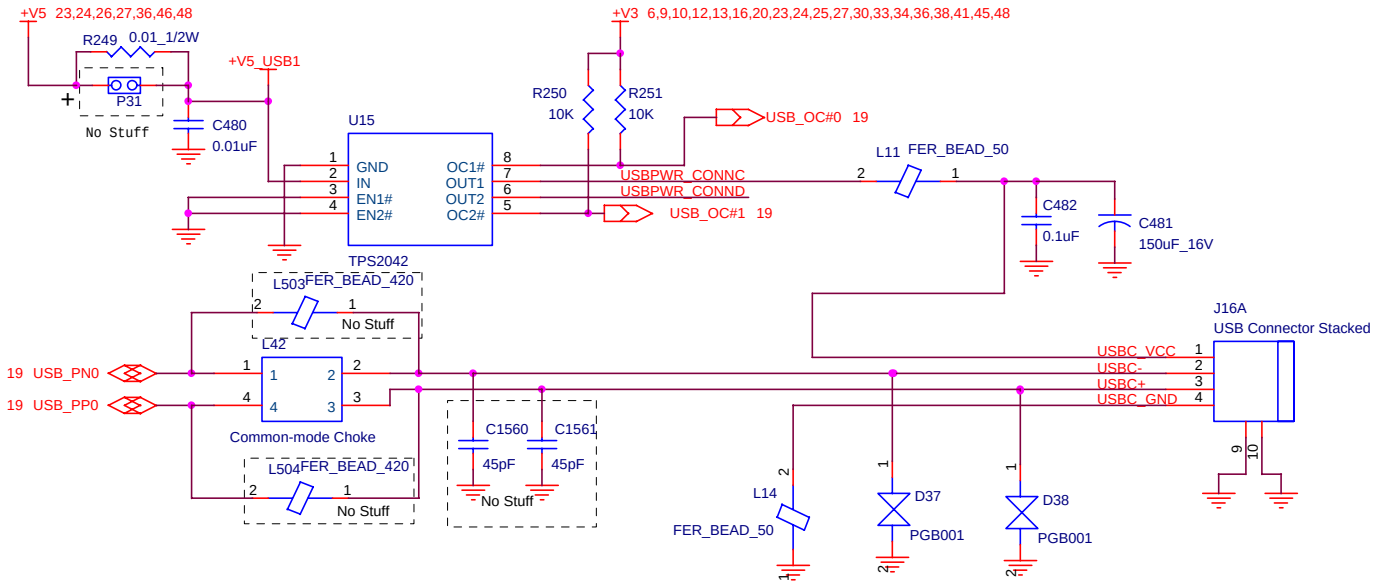

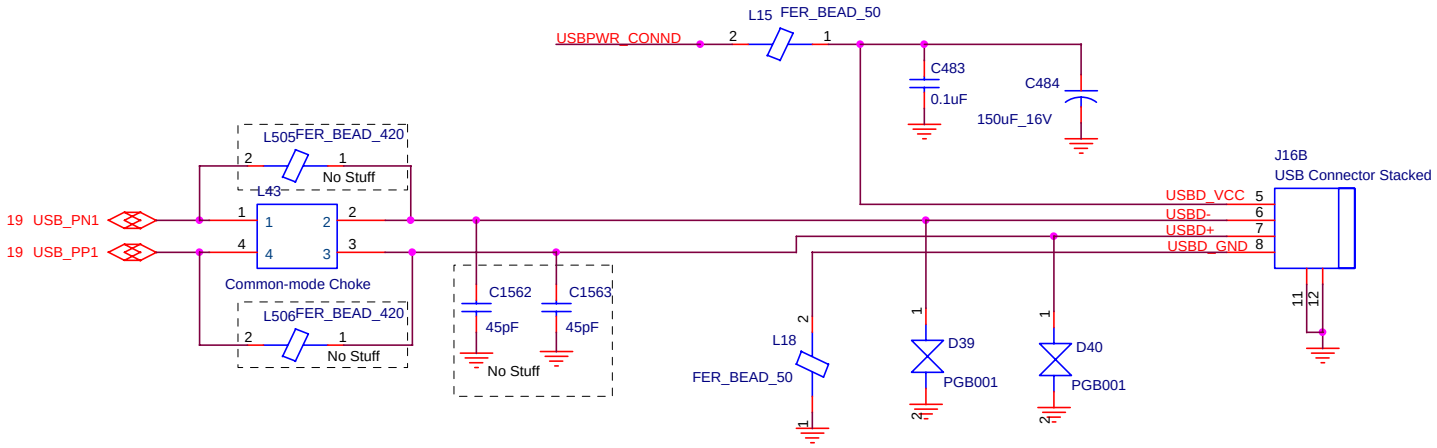

Title: USB (1 of 2)			
Size: A	Project:	Document Number	Rev
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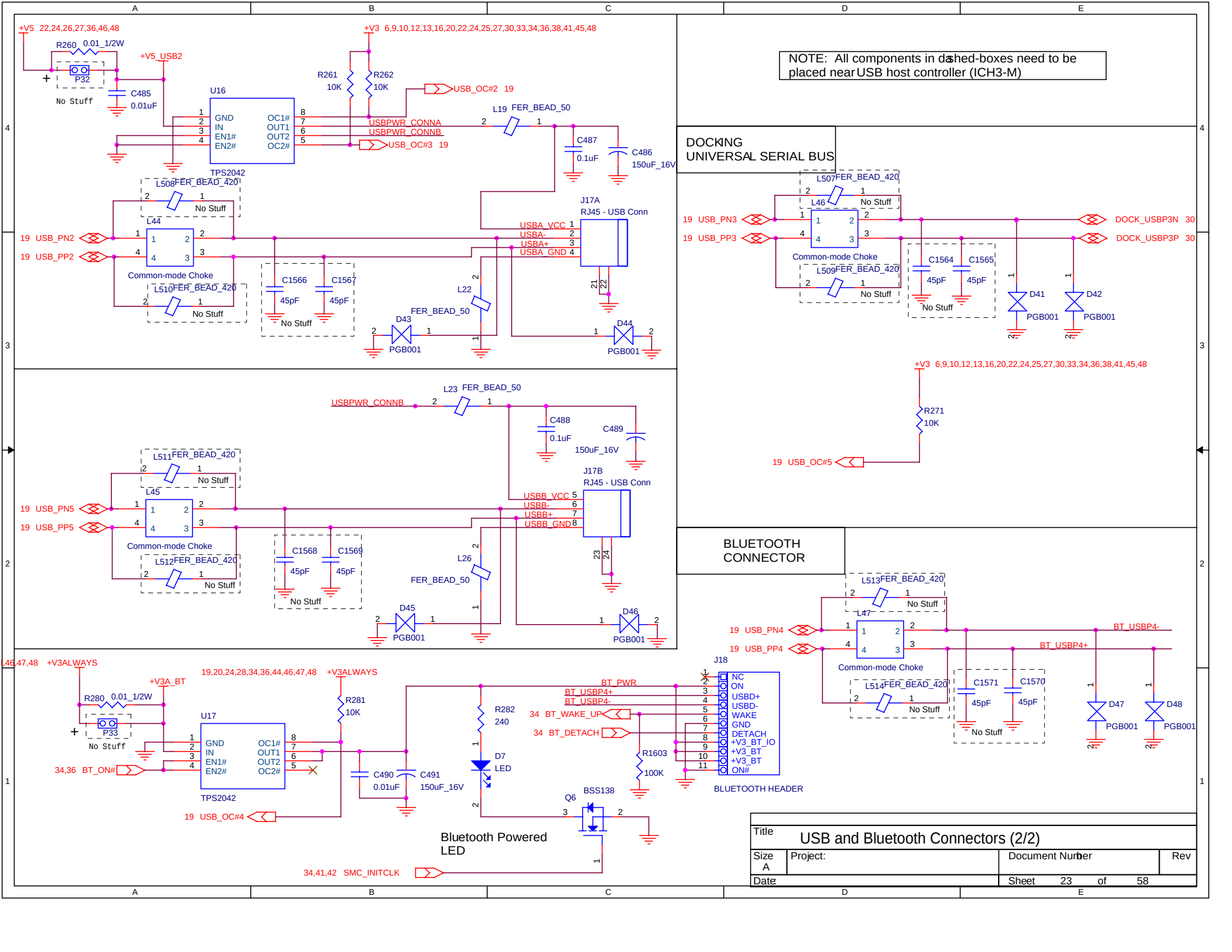
NOTE: All components in dashed-boxes need to be placed near USB host controller (ICH3-M)
DOCKING UNIVERSAL SERIAL BUS
BLUETOOTH CONNECTOR
Bluetooth Powered LED
BLUETOOTH HEADER
TPS2042
Common-mode Choke
Title
USB and Bluetooth Connectors (2/2)
Size A
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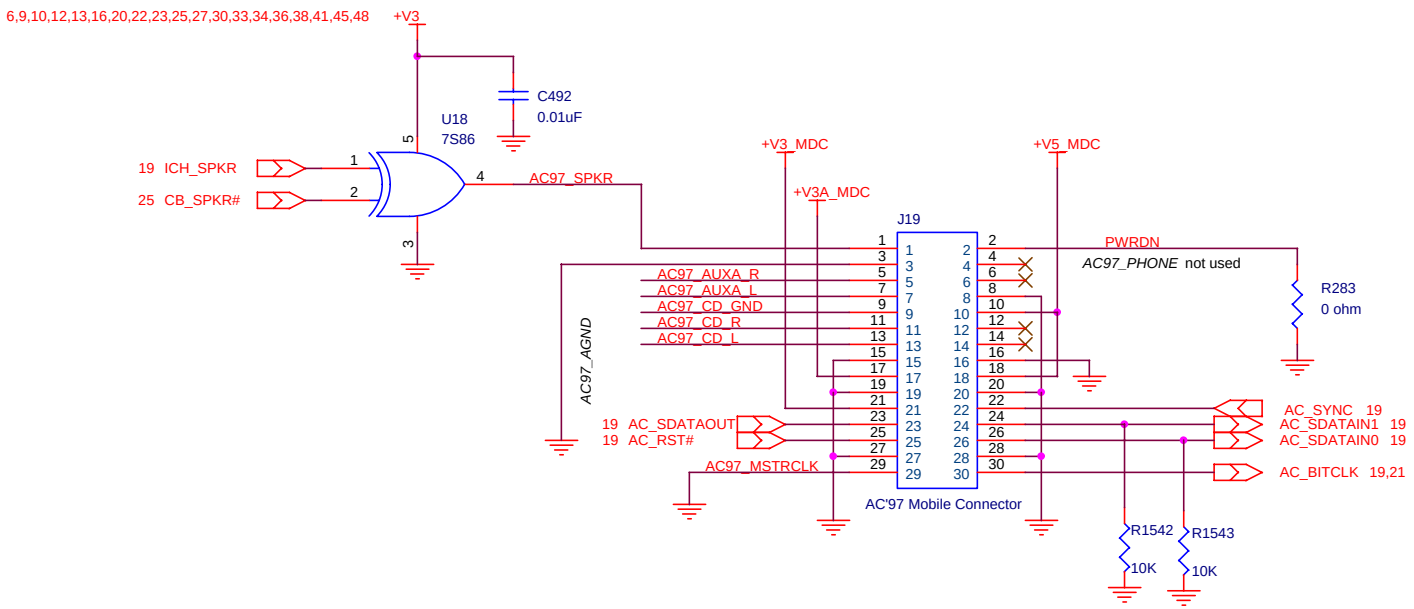
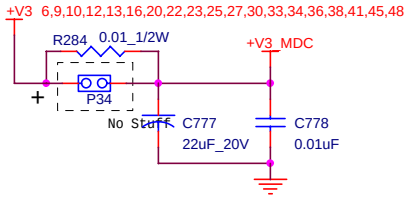
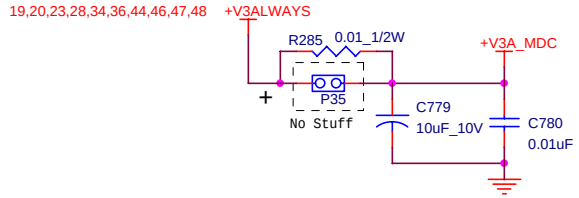
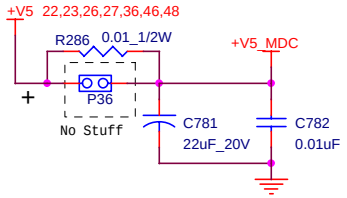
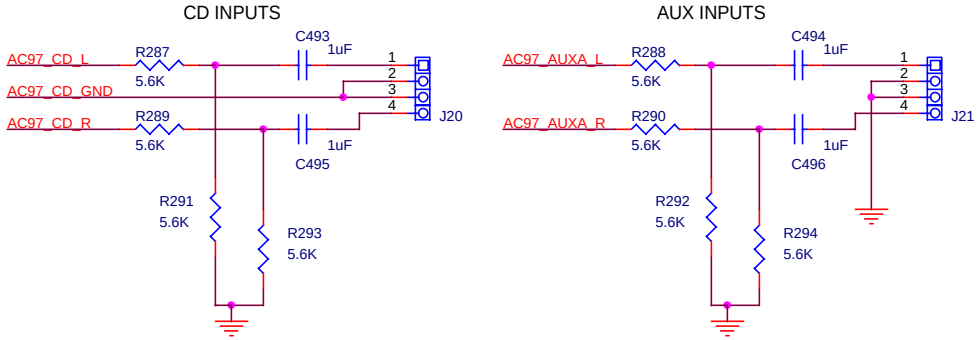
AC'97 Mobile Daughter Card Connector











Title	AC'97 & Audio Connectors		
Size A	Project:	Document Number	Rev
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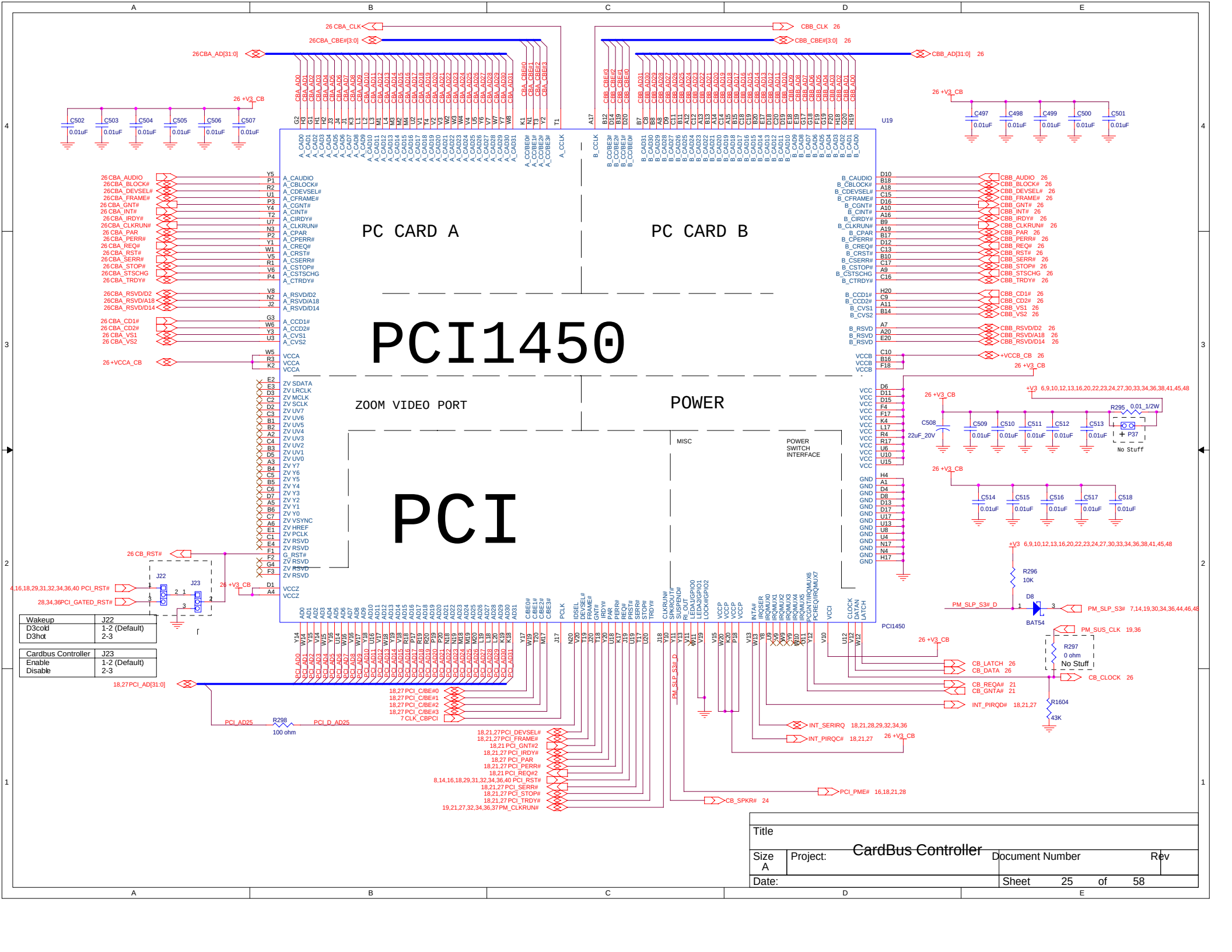
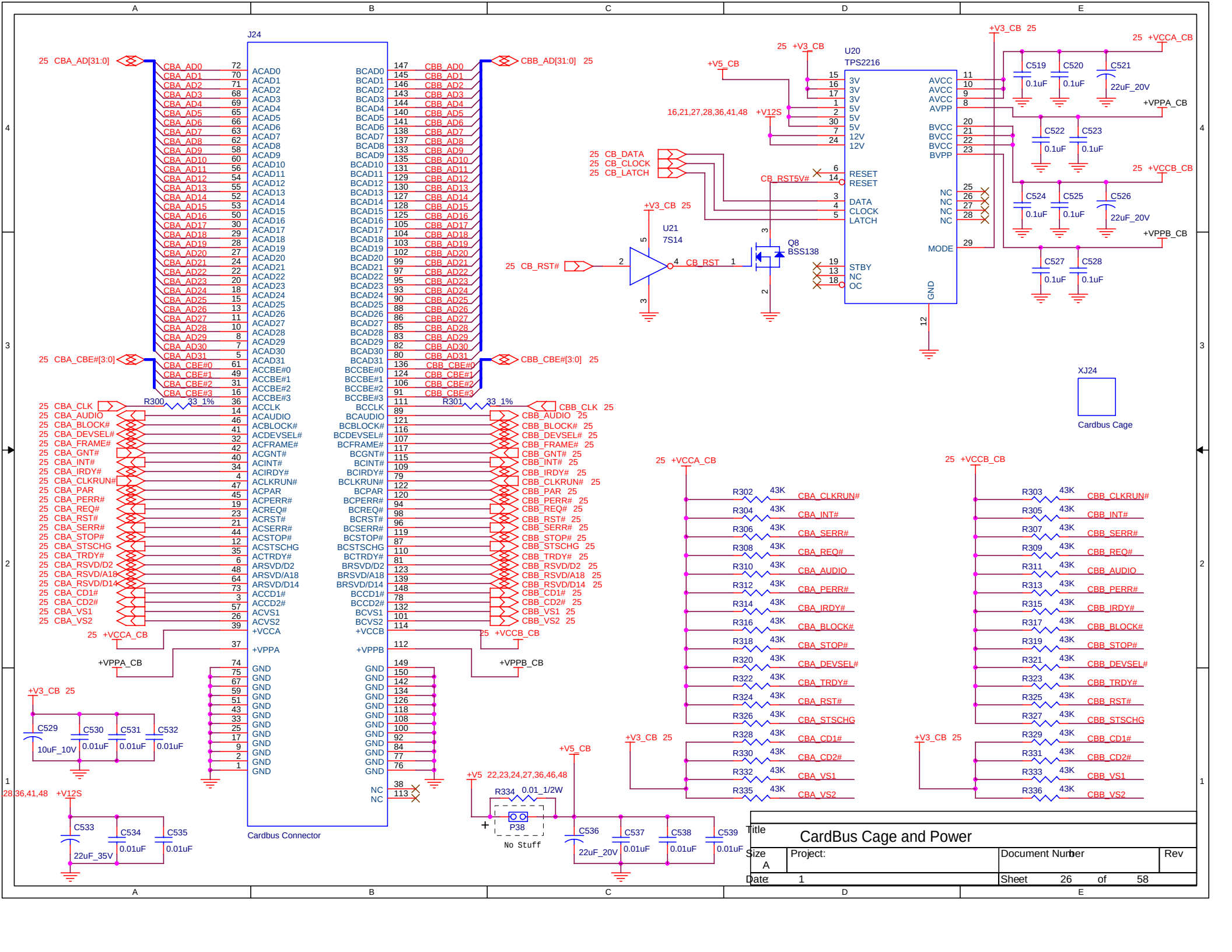

PCI1450
PC CARD A
PC CARD B
ZOOM VIDEO PORT
POWER
MISC
POWER SWITCH INTERFACE
PCI
PCI1450
U19
26 CBA_CLK
26CBA_CBE#[3:0]
26CBA_AD[31:0]
CBB_CLK 26
CBB_CBE#[3:0] 26
CBB_AD[31:0] 26
26 +V3_CB
26 +VCCA_CB
+VCCB_CB 26
+V3 6,9,10,12,13,16,20,22,23,24,27,30,33,34,36,38,41,45,48
26 CB_RST#
4,16,18,29,31,32,34,36,40 PCI_RST#
28,34,36PCI_GATED_RST#
18,27PCI_AD[31:0]
18,27 PCI_C/BE#0
18,27 PCI_C/BE#1
18,27 PCI_C/BE#2
18,27 PCI_C/BE#3
7 CLK_CBPCI
PCI_AD25
R298
100 ohm
PCI_D_AD25
PM_SLP_S3# 7,14,19,30,34,36,44,46,48
PM_SUS_CLK 19,36
CB_LATCH 26
CB_DATA 26
CB_REQA# 21
CB_GNTA# 21
INT_PIRQD# 18,21,27
CB_CLOCK 26
INT_SERIRQ 18,21,28,29,32,34,36
INT_PIRQC# 18,21,27
PCI_PME# 16,18,21,28
CB_SPKR# 24
18,21,27PCI_DEVSEL#
18,21,27PCI_FRAME#
18,21 PCI_GNT#2
18,21,27 PCI_IRDY#
18,27 PCI_PAR
18,21,27 PCI_PERR#
18,21 PCI_REQ#2
8,14,16,18,29,31,32,34,36,40 PCI_RST#
18,21,27 PCI_SERR#
18,21,27 PCI_STOP#
18,21,27 PCI_TRDY#
19,21,27,32,34,36,37PM_CLKRUN#
Wakeup | J22
D3cold | 1-2 (Default)
D3hot | 2-3
Cardbus Controller | J23
Enable | 1-2 (Default)
Disable | 2-3
Title
Size A
Project: CardBus Controller
Document Number
Rev
Date:
Sheet 25 of 58


J24
Cardbus Connector
U20
TPS2216
U21
7S14
Q8
BSS138
XJ24
Cardbus Cage
R300 33 1%
R301 33 1%
R302 43K
R303 43K
R304 43K
R305 43K
R306 43K
R307 43K
R308 43K
R309 43K
R310 43K
R311 43K
R312 43K
R313 43K
R314 43K
R315 43K
R316 43K
R317 43K
R318 43K
R319 43K
R320 43K
R321 43K
R322 43K
R323 43K
R324 43K
R325 43K
R326 43K
R327 43K
R328 43K
R329 43K
R330 43K
R331 43K
R332 43K
R333 43K
R334 0.01_1/2W
R335 43K
R336 43K
P38
No Stuff
C519 C520 C521 0.1uF 0.1uF 22uF_20V
C522 C523 0.1uF 0.1uF
C524 C525 C526 0.1uF 0.1uF 22uF_20V
C527 C528 0.1uF 0.1uF
C529 C530 C531 C532 10uF_10V 0.01uF 0.01uF 0.01uF
C533 C534 C535 22uF_35V 0.01uF 0.01uF
C536 C537 C538 C539 22uF_20V 0.01uF 0.01uF 0.01uF
Title
CardBus Cage and Power
Size A
Project:
Document Number
Rev
Date: 1
Sheet 26 of 58

Integrated diode in CBTD_16210
device provides correct voltage drop
for 5V to 3.3V translation

18,25 PCI_AD[31:0]

12,14,15,16,20,29,32,33,35,40,41,42,43,44,45,46,48 +V5S

C540 0.01uF
C541 22uF_20V 20V

U23
CBTD16210

		1	NC	VCC	15	
	U23_1A1	2	1A1	1B1	46	U23_1B1
18,21,25 PCI_FRAME#		3	1A2	1B2	45	SLT_FRAME# 28,29
18,21,25 PCI_IRDY#		4	1A3	1B3	44	SLT_IRDY# 28,29
18,21,25 PCI_TRDY#		5	1A4	1B4	43	SLT_TRDY# 28,29
18,21,25 PCI_DEVSEL#		6	1A5	1B5	42	SLT_DEVSEL# 28,29
18,21,25 PCI_STOP#		7	1A6	1B6	40	SLT_STOP# 28,29
18,21 PCI_LOCK#		9	1A7	1B7	39	SLT_LOCK# 28,29
18,21,25 PCI_PERR#		10	1A8	1B8	38	SLT_PERR# 28
18,21,25 PCI_SERR#		11	1A9	1B9	37	SLT_SERR# 28,29
18,25 PCI_PAR		12	1A10	1B10	36	SLT_PAR 28,29
19,21,25,32,34,36,37 PM_CLKRUN#		13	2A1	2B1	35	SLT_CLKRUN# 28,29
	U23_2A2	14	2A2	2B2	34	U23_2B2
18,25 PCI_C/BE#0		16	2A3	2B3	33	SLT_C/BE0# 28,29
18,25 PCI_C/BE#1		18	2A4	2B4	31	SLT_C/BE1# 28,29
18,25 PCI_C/BE#2		19	2A5	2B5	30	SLT_C/BE2# 28,29
18,25 PCI_C/BE#3		20	2A6	2B6	29	SLT_C/BE3# 28,29
16,18,21 INT_PIRQA#		21	2A7	2B7	28	SLT_IRQA# 28,29
16,18,21 INT_PIRQB#		22	2A8	2B8	27	SLT_IRQB# 28,29
18,21,25 INT_PIRQC#		23	2A9	2B9	26	SLT_IRQC# 28,29
18,21,25 INT_PIRQD#		24	2A10	2B10	25	SLT_IRQD# 28,29
		48	1OE#	GND	8	
		47	2OE#	GND	17	
				GND	32	
				GND	41	

12,14,15,16,20,29,32,33,35,40,41,42,43,44,45,46,48 +V5S

C542 0.01uF

U24
CBTD16210

		1	NC	VCC	15	
PCI_AD0		2	1A1	1B1	46	SLT_AD0
PCI_AD1		3	1A2	1B2	45	SLT_AD1
PCI_AD2		4	1A3	1B3	44	SLT_AD2
PCI_AD3		5	1A4	1B4	43	SLT_AD3
PCI_AD4		6	1A5	1B5	42	SLT_AD4
PCI_AD5		7	1A6	1B6	40	SLT_AD5
PCI_AD6		9	1A7	1B7	39	SLT_AD6
PCI_AD7		10	1A8	1B8	38	SLT_AD7
PCI_AD8		11	1A9	1B9	37	SLT_AD8
PCI_AD9		12	1A10	1B10	36	SLT_AD9
PCI_AD10		13	2A1	2B1	35	SLT_AD10
PCI_AD11		14	2A2	2B2	34	SLT_AD11
PCI_AD12		16	2A3	2B3	33	SLT_AD12
PCI_AD13		18	2A4	2B4	31	SLT_AD13
PCI_AD14		19	2A5	2B5	30	SLT_AD14
PCI_AD15		20	2A6	2B6	29	SLT_AD15
PCI_AD16		21	2A7	2B7	28	SLT_AD16
PCI_AD17		22	2A8	2B8	27	SLT_AD17
PCI_AD18		23	2A9	2B9	26	SLT_AD18
PCI_AD19		24	2A10	2B10	25	SLT_AD19
		48	1OE#	GND	8	
		47	2OE#	GND	17	
				GND	32	
				GND	41	

+V5S 12,14,15,16,20,29,32,33,35,40,41,42,

C543 0.01uF

U22
CBTD16210

		1	NC	VCC	15	
PCI_AD20		2	1A1	1B1	46	SLT_AD20
PCI_AD21		3	1A2	1B2	45	SLT_AD21
PCI_AD22		4	1A3	1B3	44	SLT_AD22
PCI_AD23		5	1A4	1B4	43	SLT_AD23
PCI_AD24		6	1A5	1B5	42	SLT_AD24
PCI_AD25		7	1A6	1B6	40	SLT_AD25
PCI_AD26		9	1A7	1B7	39	SLT_AD26
PCI_AD27		10	1A8	1B8	38	SLT_AD27
PCI_AD28		11	1A9	1B9	37	SLT_AD28
PCI_AD29		12	1A10	1B10	36	SLT_AD29
PCI_AD30		13	2A1	2B1	35	SLT_AD30
PCI_AD31		14	2A2	2B2	34	SLT_AD31
U22_2A3		16	2A3	2B3	33	U22_2B3
U22_2A4		18	2A4	2B4	31	U22_2B4
U22_2A5		19	2A5	2B5	30	U22_2B5
U22_2A6		20	2A6	2B6	29	U22_2B6
18,21 PCI_REQ#3		21	2A7	2B7	28	SLT_REQ#3 28
18 PCI_GNT#3		22	2A8	2B8	27	SLT_GNT#3 28
18,21 PCI_REQ#0		23	2A9	2B9	26	SLT_REQ#0 28
18 PCI_GNT#0		24	2A10	2B10	25	SLT_GNT#0 28
		48	1OE#	GND	8	
		47	2OE#	GND	17	
				GND	32	
				GND	41	

SLT_AD[31:0] 28,29

+V5 22,23,24,26,36,46,48
28 +V5_SLT
R337 0.01_1/2W
P39
No Stuff

C544 22uF_20V 20V
C545 22uF_20V 20V
C546 22uF_20V 20V
C547 22uF_20V 20V
C548 0.01uF
C549 0.01uF
C550 0.01uF
C551 0.01uF
C552 0.01uF
C553 0.01uF
C554 0.01uF
C555 0.01uF
C556 0.01uF
C557 0.01uF
C558 0.01uF
C559 0.01uF
C560 0.01uF
C561 0.01uF

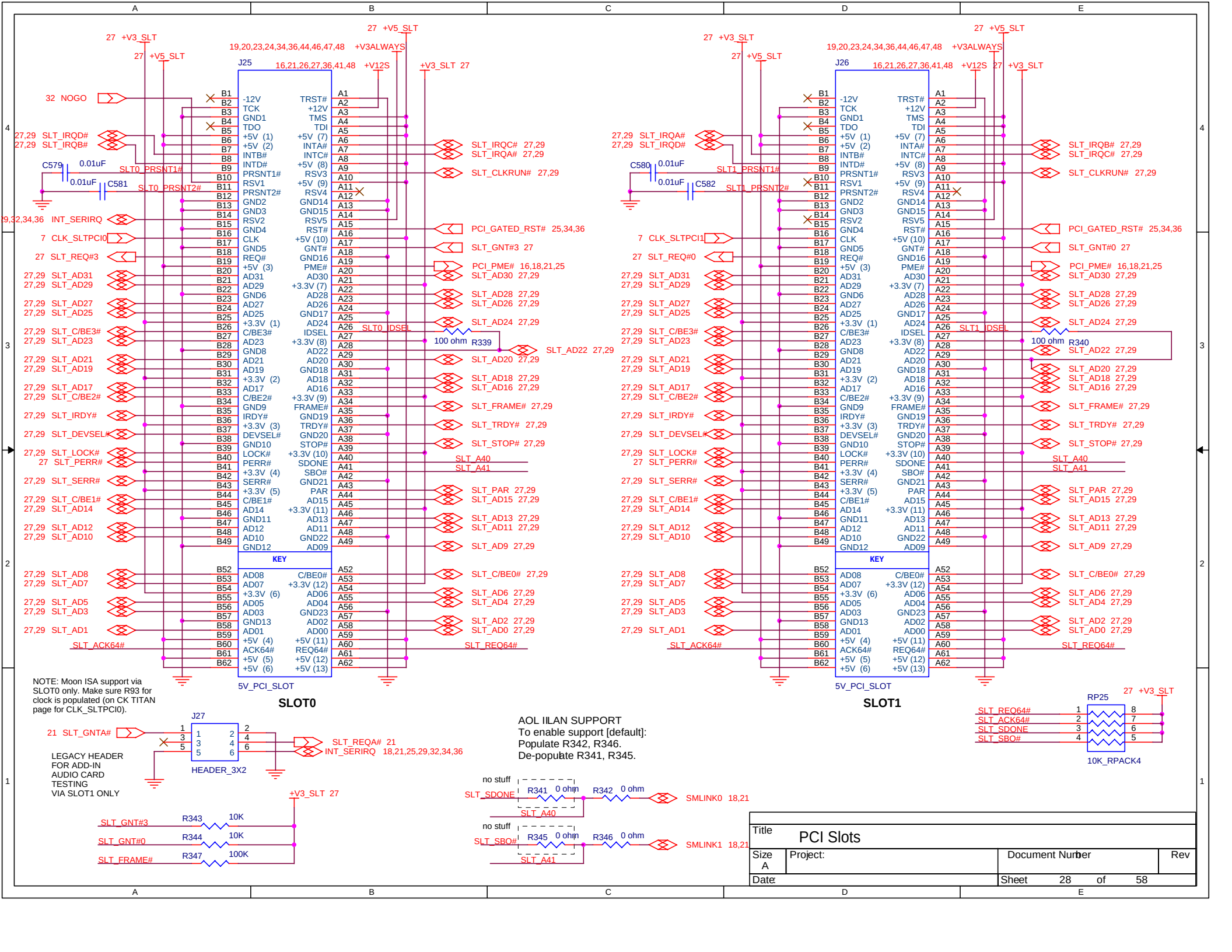
+V3 6,9,10,12,13,16,20,22,23,24,25,30,33,34,36,38,41,45,48
28 +V3_SLT
R338 0.01_1/2W
P40
No Stuff

C562 22uF_20V 20V
C563 22uF_20V 20V
C564 0.01uF
C565 0.01uF
C566 0.01uF
C567 0.01uF
C568 0.01uF
C569 0.01uF
C570 0.01uF
C571 0.01uF
C572 0.01uF
C573 0.01uF
C574 0.01uF
C575 0.01uF

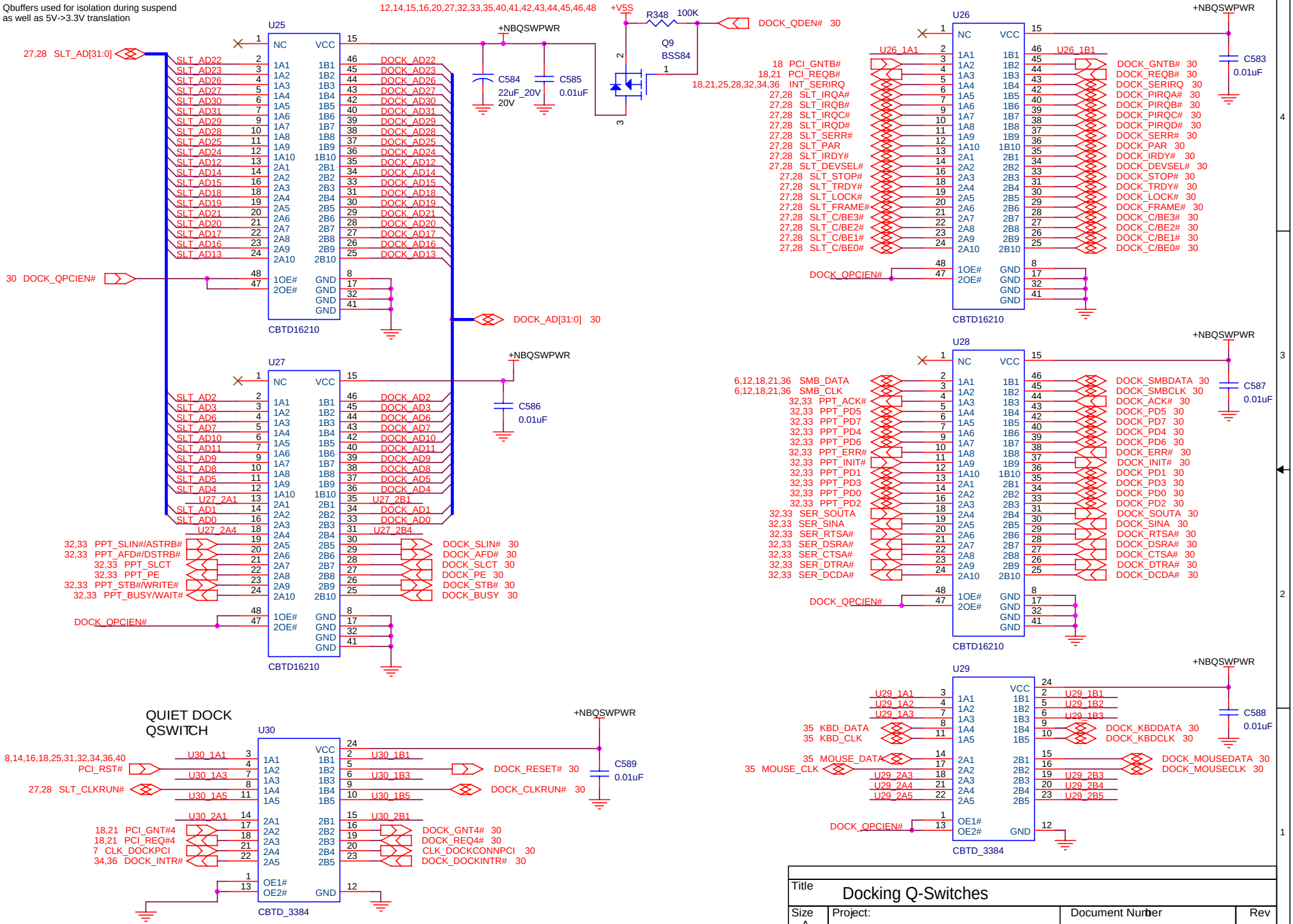
16,21,26,28,36,41,48 +V12S

C576 22uF_35V
C577 0.01uF
C578 0.01uF

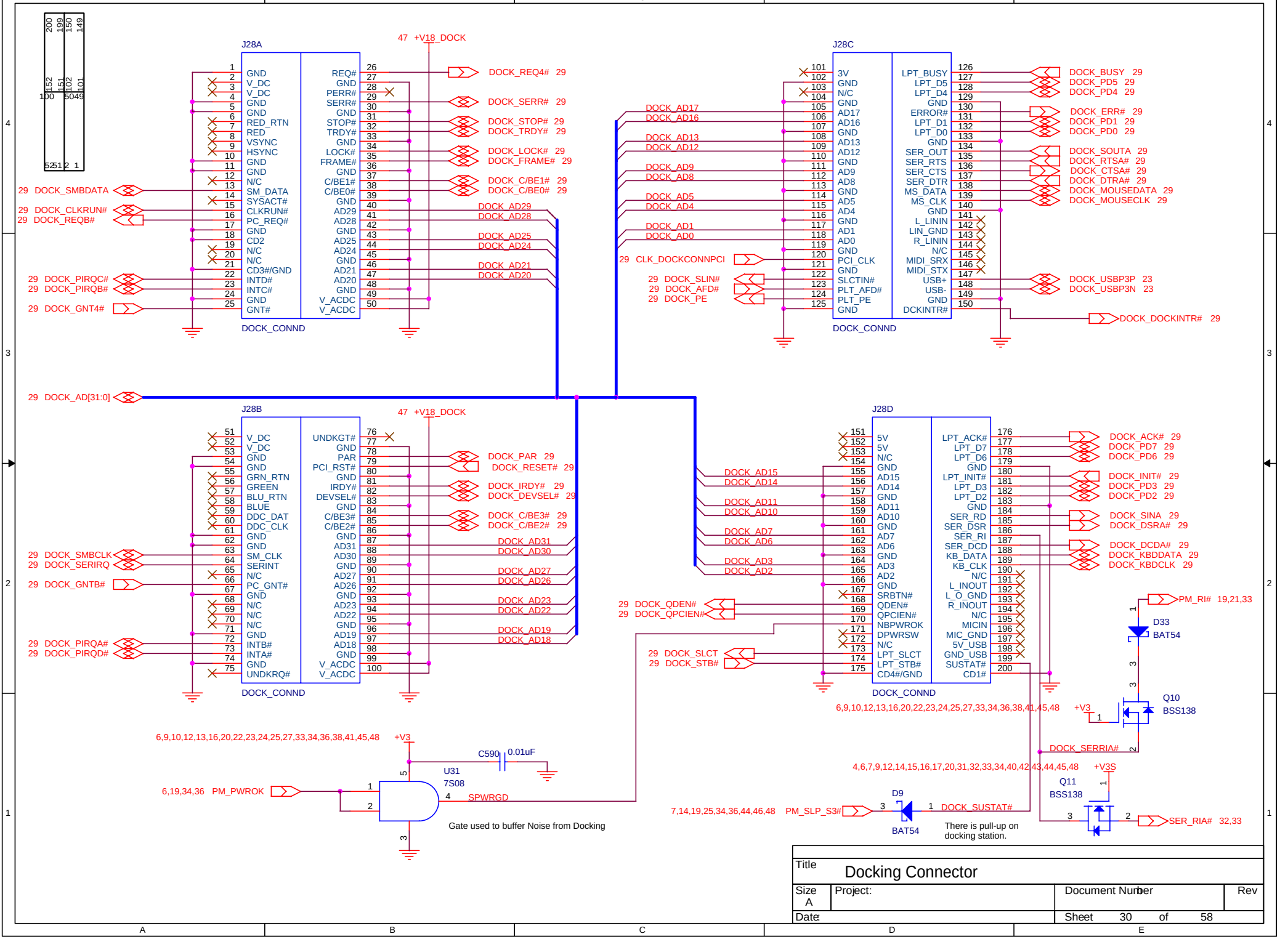
Title	PCI Q-Switches and Decoupling		
Size A	Project: A	Document Number	Rev
Date		Sheet 27 of 58	


SLOT0
SLOT1
5V_PCI_SLOT
J25
J26
J27
KEY
NOTE: Moon ISA support via SLOT0 only. Make sure R93 for clock is populated (on CK TITAN page for CLK_SLTPCI0).
LEGACY HEADER FOR ADD-IN AUDIO CARD TESTING VIA SLOT1 ONLY
HEADER_3X2
AOL IILAN SUPPORT
To enable support [default]:
Populate R342, R346.
De-populate R341, R345.
no stuff
RP25
10K_RPACK4
Title
PCI Slots
Size
A
Project:
Document Number
Rev
Date:
Sheet 28 of 58

Qbuffers used for isolation during suspend
as well as 5V->3.3V translation



Title	Docking Q-Switches		
Size A	Project:	Document Number	Rev
Date		Sheet 29 of 58	


J28A
J28B
J28C
J28D
DOCK_CONND
47 +V18_DOCK
29 DOCK_AD[31:0]
29 DOCK_SMBDATA
29 DOCK_CLKRUN#
29 DOCK_REQB#
29 DOCK_PIRQC#
29 DOCK_PIRQB#
29 DOCK_GNT4#
29 DOCK_SMBCLK
29 DOCK_SERIRQ
29 DOCK_GNTB#
29 DOCK_PIRQA#
29 DOCK_PIRQD#
DOCK_REQ4# 29
DOCK_SERR# 29
DOCK_STOP# 29
DOCK_TRDY# 29
DOCK_LOCK# 29
DOCK_FRAME# 29
DOCK_C/BE1# 29
DOCK_C/BE0# 29
DOCK_PAR 29
DOCK_RESET# 29
DOCK_IRDY# 29
DOCK_DEVSEL# 29
DOCK_C/BE3# 29
DOCK_C/BE2# 29
29 CLK_DOCKCONNPCI
29 DOCK_SLIN#
29 DOCK_AFD#
29 DOCK_PE
DOCK_BUSY 29
DOCK_PD5 29
DOCK_PD4 29
DOCK_ERR# 29
DOCK_PD1 29
DOCK_PD0 29
DOCK_SOUTA 29
DOCK_RTSA# 29
DOCK_CTSA# 29
DOCK_DTRA# 29
DOCK_MOUSEDATA 29
DOCK_MOUSECLK 29
DOCK_USBP3P 23
DOCK_USBP3N 23
DOCK_DOCKINTR# 29
29 DOCK_QDEN#
29 DOCK_QPCIEN#
29 DOCK_SLCT
29 DOCK_STB#
DOCK_ACK# 29
DOCK_PD7 29
DOCK_PD6 29
DOCK_INIT# 29
DOCK_PD3 29
DOCK_PD2 29
DOCK_SINA 29
DOCK_DSRA# 29
DOCK_DCDA# 29
DOCK_KBDDATA 29
DOCK_KBDCLK 29
6,9,10,12,13,16,20,22,23,24,25,27,33,34,36,38,41,45,48 +V3
C590 0.01uF
U31
7S08
6,19,34,36 PM_PWROK
SPWRGD
Gate used to buffer Noise from Docking
PM_RI# 19,21,33
D33
BAT54
Q10
BSS138
DOCK_SERRIA#
4,6,7,9,12,14,15,16,17,20,31,32,33,34,40,42,43,44,45,48 +V3S
Q11
BSS138
7,14,19,25,34,36,44,46,48 PM_SLP_S3#
D9
BAT54
DOCK_SUSTAT#
There is pull-up on docking station.
SER_RIA# 32,33
Title
Docking Connector
Size A
Project:
Document Number
Rev
Date
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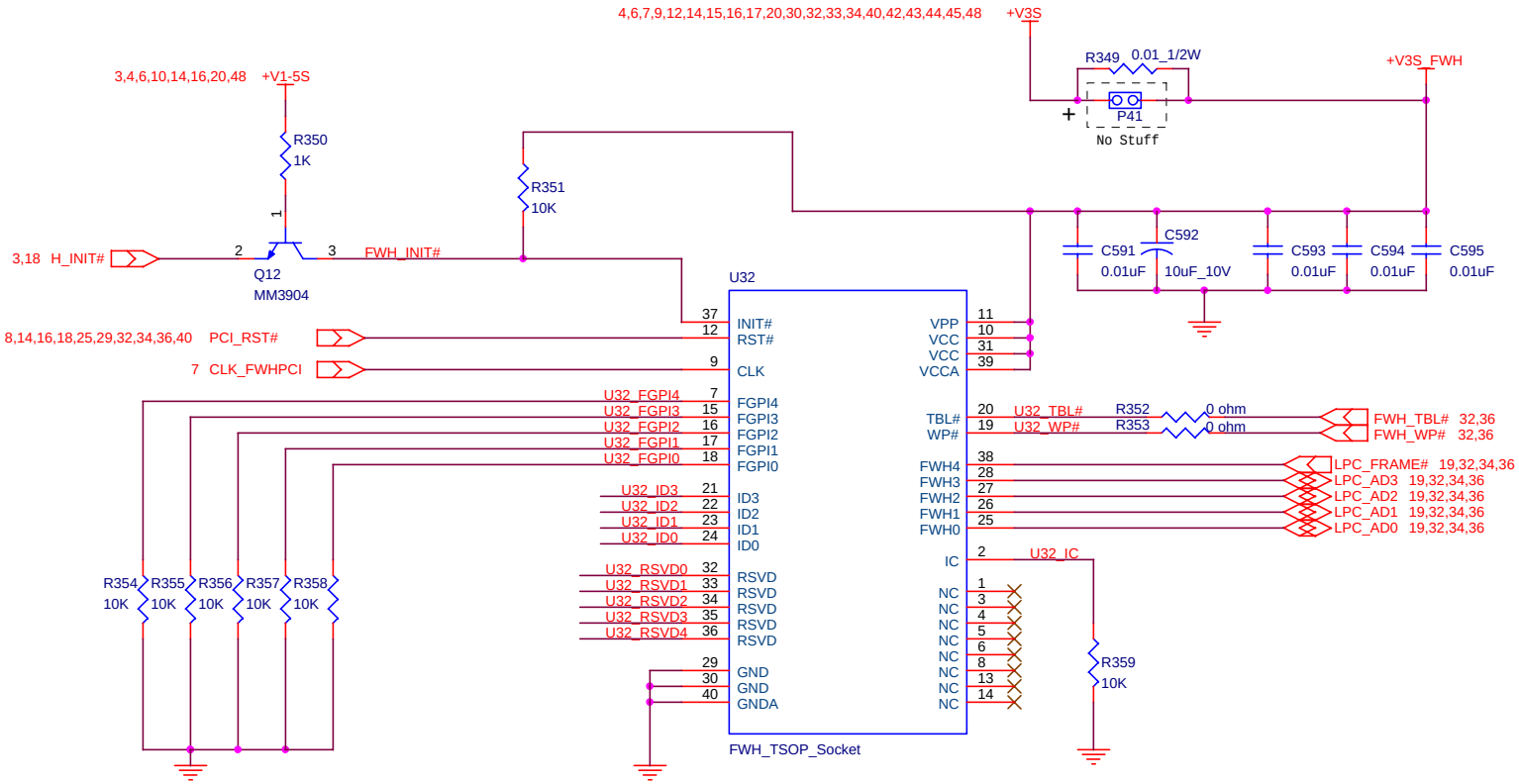
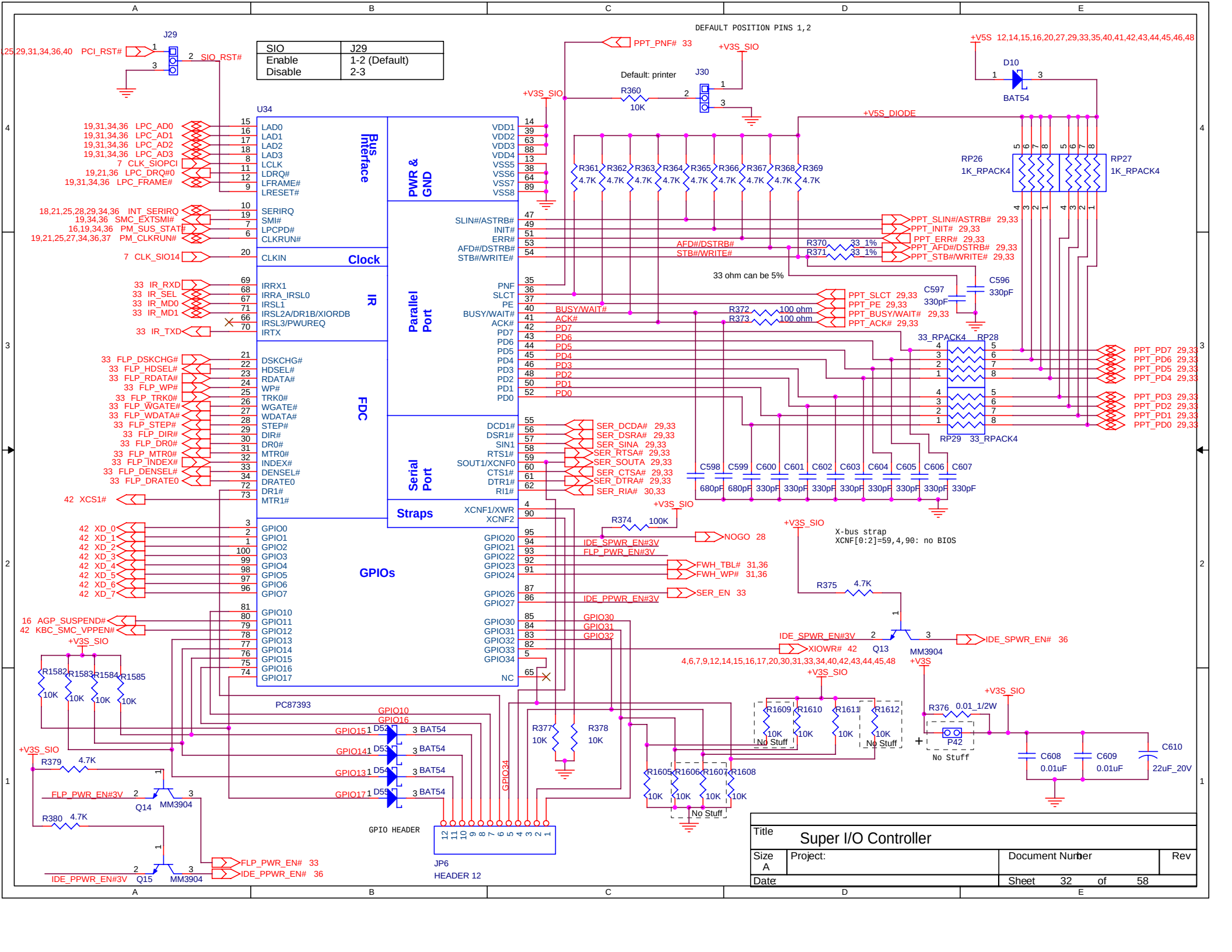


FWH sits in the FWH_TSOP_Socket, Not on the board

Title: FWH			
Size: A	Project:	Document Number	Rev
Date:		Sheet 31 of 58	


DEFAULT POSITION PINS 1,2
SIO | J29
Enable | 1-2 (Default)
Disable | 2-3
J29
PCI_RST#
SIO_RST#
U34
Bus Interface
LAD0
LAD1
LAD2
LAD3
LCLK
LDRQ#
LFRAME#
LRESET#
SERIRQ
SMI#
LPCPD#
CLKRUN#
Clock
CLKIN
IR
IRRX1
IRRA_IRSL0
IRSL1
IRSL2A/DR1B/XIORDB
IRSL3/PWUREQ
IRTX
FDC
DSKCHG#
HDSEL#
RDATA#
WP#
TRK0#
WGATE#
WDATA#
STEP#
DIR#
DR0#
MTR0#
INDEX#
DENSEL#
DRATE0
DR1#
MTR1#
GPIOs
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16
GPIO17
PWR & GND
VDD1
VDD2
VDD3
VDD4
VSS5
VSS6
VSS7
VSS8
Parallel Port
SLIN#/ASTRB#
INIT#
ERR#
AFD#/DSTRB#
STB#/WRITE#
PNF
SLCT
PE
BUSY/WAIT#
ACK#
PD7
PD6
PD5
PD4
PD3
PD2
PD1
PD0
Serial Port
DCD1#
DSR1#
SIN1
RTS1#
SOUT1/XCNF0
CTS1#
DTR1#
RI1#
Straps
XCNF1/XWR
XCNF2
GPIO20
GPIO21
GPIO22
GPIO23
GPIO24
GPIO26
GPIO27
GPIO30
GPIO31
GPIO32
GPIO33
GPIO34
NC
PC87393
GPIO HEADER
JP6
HEADER 12
PPT_PNF# 33
+V3S_SIO
Default: printer
J30
R360 10K
+V5S_DIODE
D10
BAT54
+V5S 12,14,15,16,20,27,29,33,35,40,41,42,43,44,45,46,48
R361 4.7K
R362 4.7K
R363 4.7K
R364 4.7K
R365 4.7K
R366 4.7K
R367 4.7K
R368 4.7K
R369 4.7K
RP26 1K_RPACK4
RP27 1K_RPACK4
PPT_SLIN#/ASTRB# 29,33
PPT_INIT# 29,33
PPT_ERR# 29,33
PPT_AFD#/DSTRB# 29,33
PPT_STB#/WRITE# 29,33
AFD#/DSTRB#
STB#/WRITE#
R370 33 1%
R371 33 1%
33 ohm can be 5%
C596 330pF
C597 330pF
PPT_SLCT 29,33
PPT_PE 29,33
PPT_BUSY/WAIT# 29,33
PPT_ACK# 29,33
R372 100 ohm
R373 100 ohm
BUSY/WAIT#
ACK#
PD7
PD6
PD5
PD4
PD3
PD2
PD1
PD0
33_RPACK4 RP28
RP29 33_RPACK4
PPT_PD7 29,33
PPT_PD6 29,33
PPT_PD5 29,33
PPT_PD4 29,33
PPT_PD3 29,33
PPT_PD2 29,33
PPT_PD1 29,33
PPT_PD0 29,33
SER_DCDA# 29,33
SER_DSRA# 29,33
SER_SINA 29,33
SER_RTSA# 29,33
SER_SOUTA 29,33
SER_CTSA# 29,33
SER_DTRA# 29,33
SER_RIA# 30,33
C598 680pF
C599 680pF
C600 330pF
C601 330pF
C602 330pF
C603 330pF
C604 330pF
C605 330pF
C606 330pF
C607 330pF
R374 100K
NOGO 28
IDE_SPWR_EN#3V
FLP_PWR_EN#3V
FWH_TBL# 31,36
FWH_WP# 31,36
SER_EN 33
IDE_PPWR_EN#3V
X-bus strap
XCNF[0:2]=59,4,90: no BIOS
R375 4.7K
IDE_SPWR_EN# 36
XIOWR# 42
Q13 MM3904
4,6,7,9,12,14,15,16,17,20,30,31,33,34,40,42,43,44,45,48
+V3S
R376 0.01 1/2W
P42 No Stuff
C608 0.01uF
C609 0.01uF
C610 22uF_20V
R1609 10K No Stuff
R1610 10K
R1611 10K
R1612 10K No Stuff
R1605 10K
R1606 10K
R1607 10K
R1608 10K No Stuff
R377 10K
R378 10K
R1582 10K
R1583 10K
R1584 10K
R1585 10K
R379 4.7K
R380 4.7K
Q14 MM3904
Q15 MM3904
FLP_PWR_EN# 33
IDE_PPWR_EN# 36
BAT54
GPIO10
GPIO16
GPIO15
GPIO14
GPIO13
GPIO12
GPIO34
GPIO30
GPIO31
GPIO32
XCNF[0:2]=59,4,90: no BIOS
Title
Super I/O Controller
Size A
Project:
Document Number
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Date
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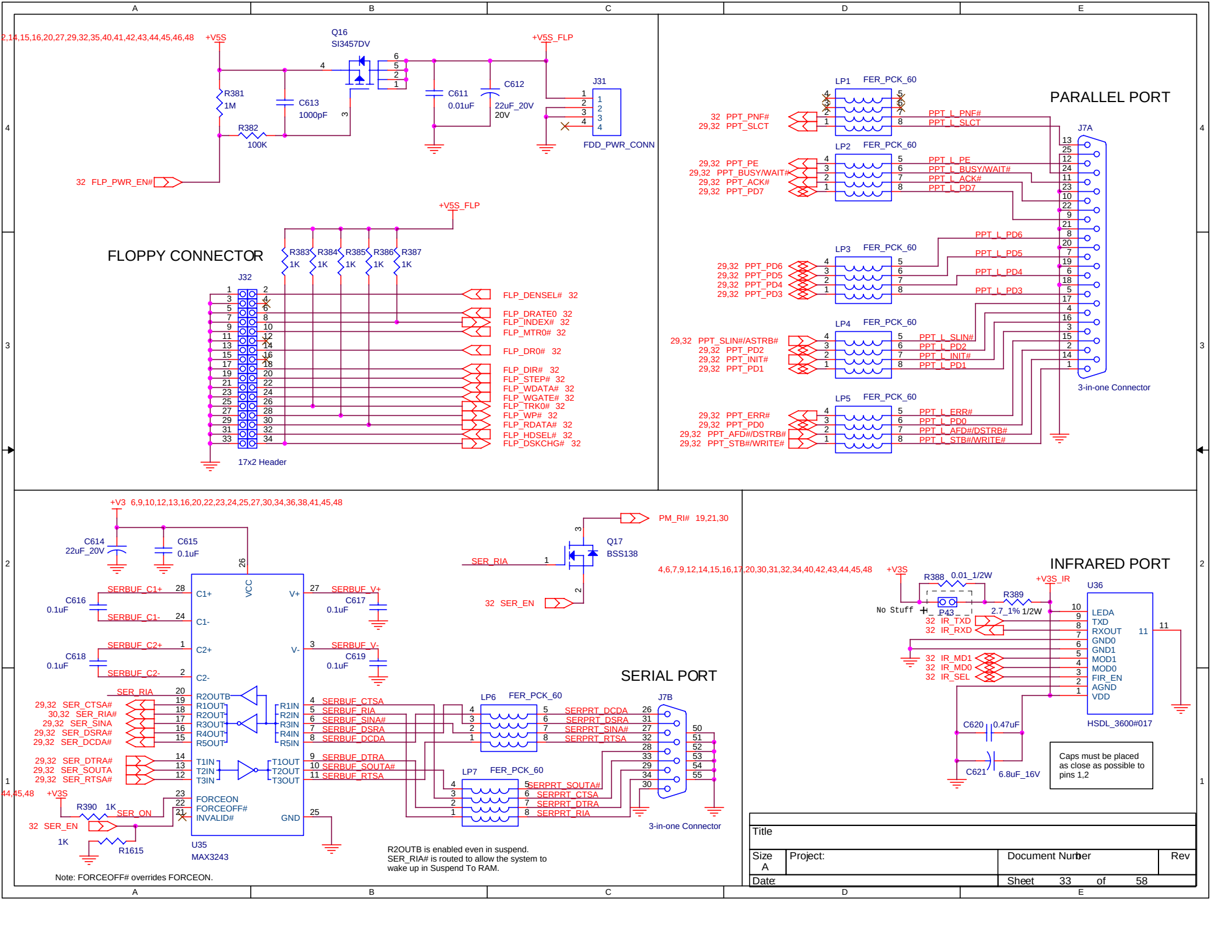
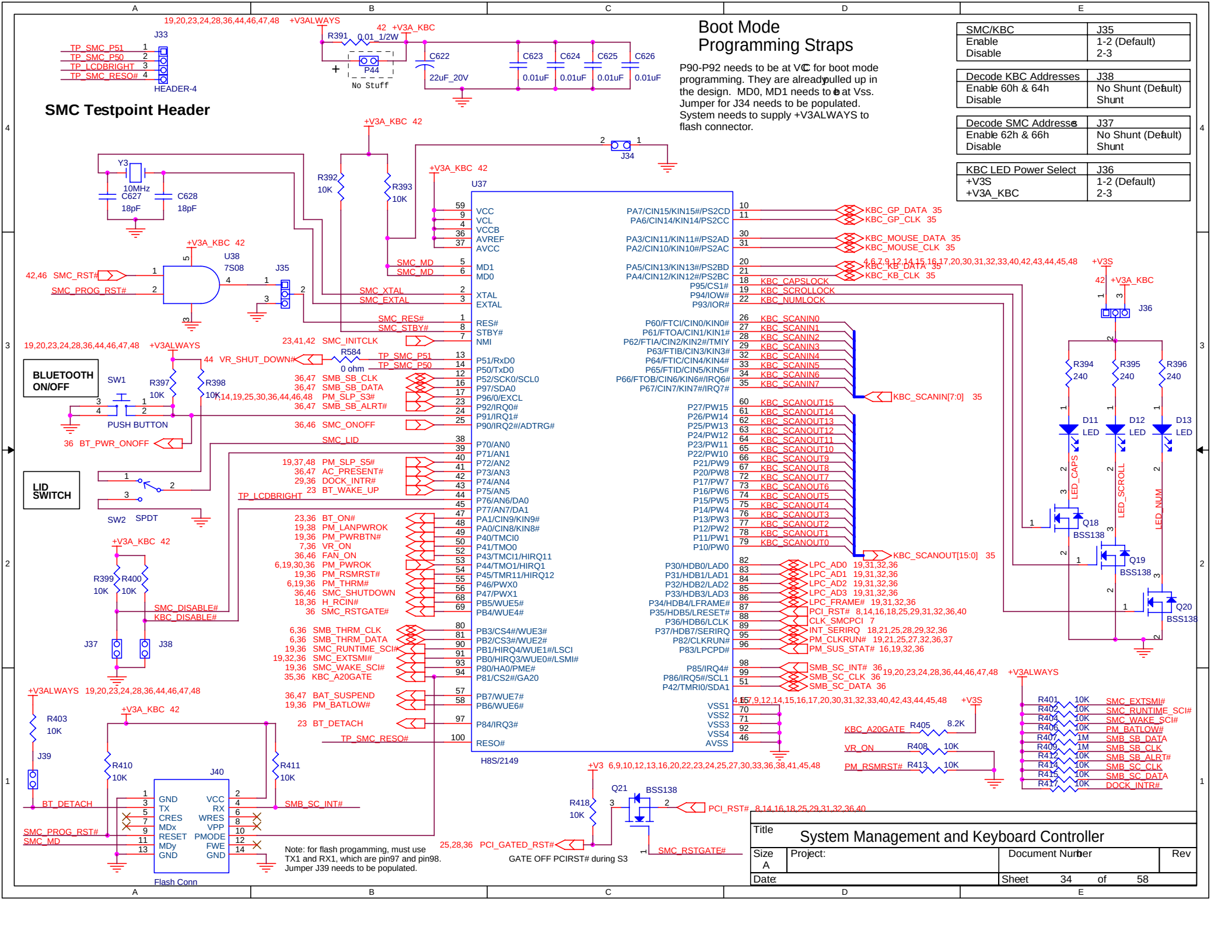
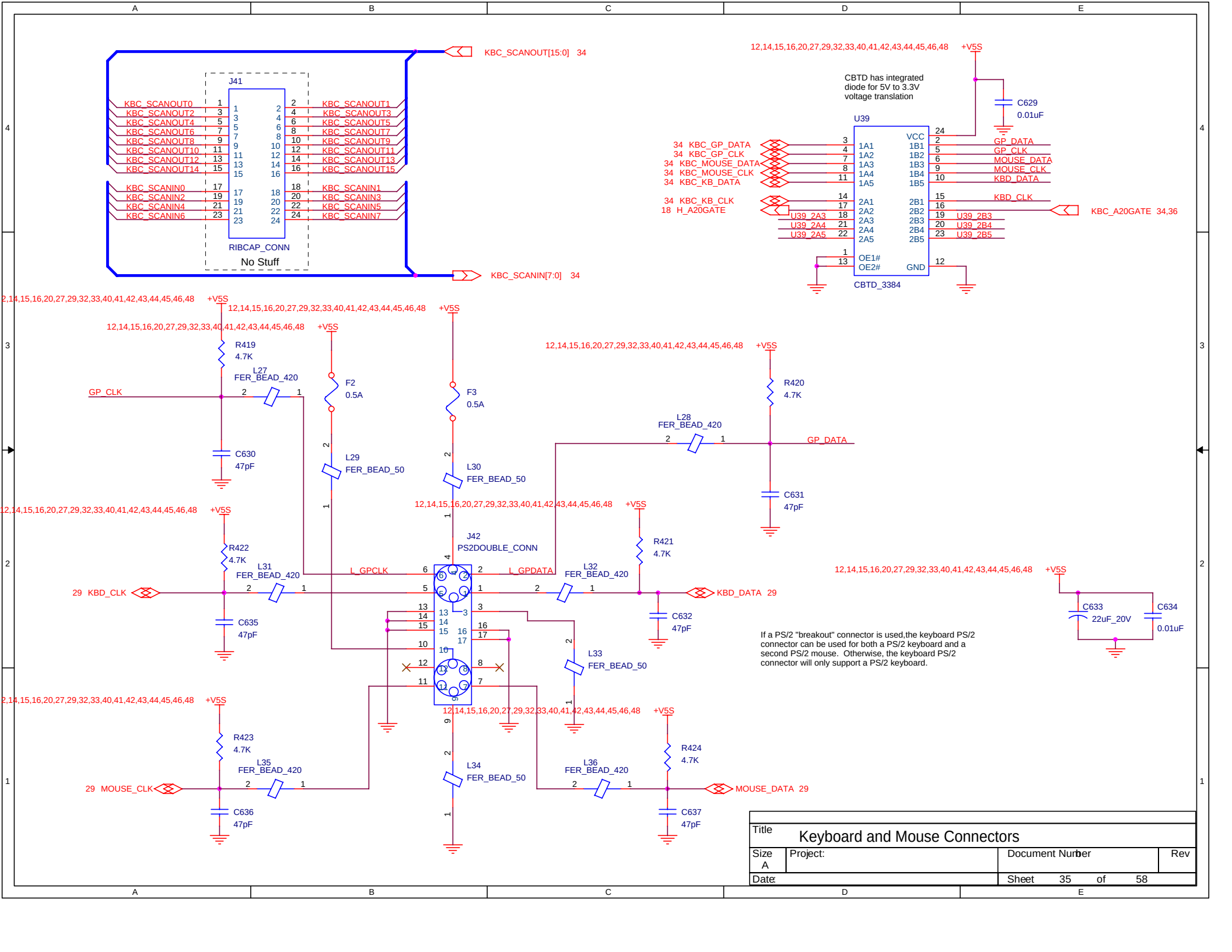
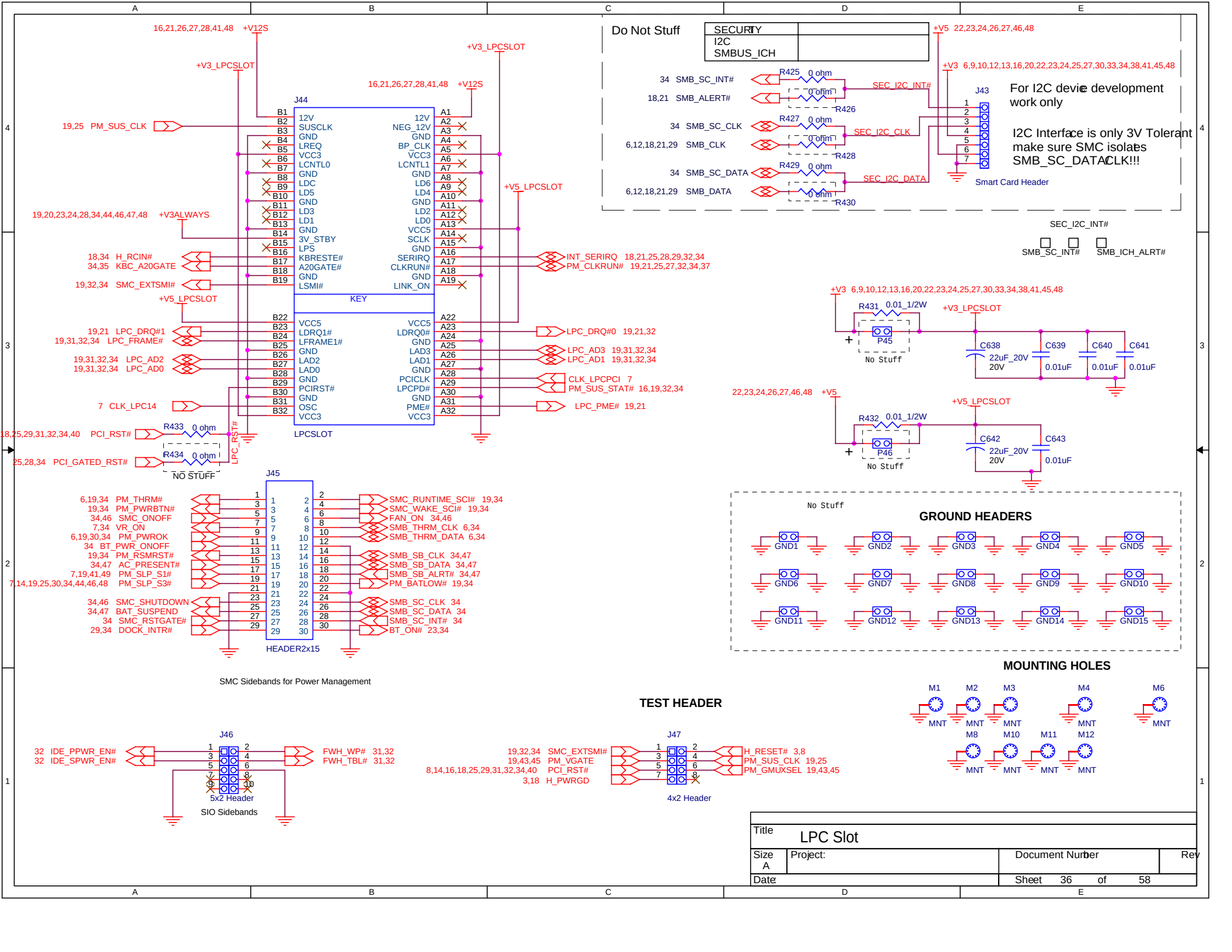
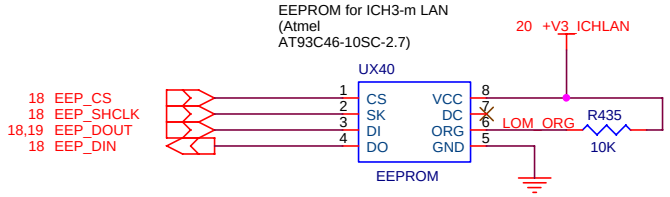
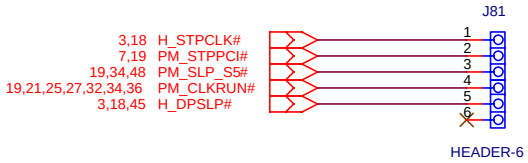

Q16
SI3457DV
+V5S
+V5S_FLP
R381
1M
R382
100K
C613
1000pF
C611
0.01uF
C612
22uF_20V
20V
J31
FDD_PWR_CONN
32 FLP_PWR_EN#
FLOPPY CONNECTOR
+V5S_FLP
R383 R384 R385 R386 R387
1K
J32
FLP_DENSEL# 32
FLP_DRATE0 32
FLP_INDEX# 32
FLP_MTR0# 32
FLP_DR0# 32
FLP_DIR# 32
FLP_STEP# 32
FLP_WDATA# 32
FLP_WGATE# 32
FLP_TRK0# 32
FLP_WP# 32
FLP_RDATA# 32
FLP_HDSEL# 32
FLP_DSKCHG# 32
17x2 Header
PARALLEL PORT
LP1 FER_PCK_60
LP2 FER_PCK_60
LP3 FER_PCK_60
LP4 FER_PCK_60
LP5 FER_PCK_60
32 PPT_PNF#
29,32 PPT_SLCT
29,32 PPT_PE
29,32 PPT_BUSY/WAIT#
29,32 PPT_ACK#
29,32 PPT_PD7
29,32 PPT_PD6
29,32 PPT_PD5
29,32 PPT_PD4
29,32 PPT_PD3
29,32 PPT_SLIN#/ASTRB#
29,32 PPT_PD2
29,32 PPT_INIT#
29,32 PPT_PD1
29,32 PPT_ERR#
29,32 PPT_PD0
29,32 PPT_AFD#/DSTRB#
29,32 PPT_STB#/WRITE#
PPT_L_PNF#
PPT_L_SLCT
PPT_L_PE
PPT_L_BUSY/WAIT#
PPT_L_ACK#
PPT_L_PD7
PPT_L_PD6
PPT_L_PD5
PPT_L_PD4
PPT_L_PD3
PPT_L_SLIN#
PPT_L_PD2
PPT_L_INIT#
PPT_L_PD1
PPT_L_ERR#
PPT_L_PD0
PPT_L_AFD#/DSTRB#
PPT_L_STB#/WRITE#
J7A
3-in-one Connector
+V3 6,9,10,12,13,16,20,22,23,24,25,27,30,34,36,38,41,45,48
C614
22uF_20V
C615
0.1uF
C616
C617
C618
C619
SERBUF_C1+
SERBUF_C1-
SERBUF_C2+
SERBUF_C2-
SERBUF_V+
SERBUF_V-
SER_RIA
VCC
C1+
C1-
C2+
C2-
V+
V-
R2OUTB
R1OUT
R2OUT
R3OUT
R4OUT
R5OUT
R1IN
R2IN
R3IN
R4IN
R5IN
T1IN
T2IN
T3IN
T1OUT
T2OUT
T3OUT
FORCEON
FORCEOFF#
INVALID#
GND
U35
MAX3243
29,32 SER_CTSA#
30,32 SER_RIA#
29,32 SER_SINA
29,32 SER_DSRA#
29,32 SER_DCDA#
29,32 SER_DTRA#
29,32 SER_SOUTA
29,32 SER_RTSA#
SERBUF_CTSA
SERBUF_RIA
SERBUF_SINA#
SERBUF_DSRA
SERBUF_DCDA
SERBUF_DTRA
SERBUF_SOUTA#
SERBUF_RTSA
R390 1K
SER_ON
32 SER_EN
1K
R1615
Note: FORCEOFF# overrides FORCEON.
PM_RI# 19,21,30
Q17
BSS138
SER_RIA
32 SER_EN
SERIAL PORT
LP6 FER_PCK_60
LP7 FER_PCK_60
SERPRT_DCDA
SERPRT_DSRA
SERPRT_SINA#
SERPRT_RTSA
SERPRT_SOUTA#
SERPRT_CTSA
SERPRT_DTRA
SERPRT_RIA
J7B
3-in-one Connector
R2OUTB is enabled even in suspend.
SER_RIA# is routed to allow the system to
wake up in Suspend To RAM.
4,6,7,9,12,14,15,16,17,20,30,31,32,34,40,42,43,44,45,48
+V3S
+V3S_IR
R388 0.01_1/2W
R389
2.7_1% 1/2W
No Stuff
P43
32 IR_TXD
32 IR_RXD
32 IR_MD1
32 IR_MD0
32 IR_SEL
INFRARED PORT
U36
LEDA
TXD
RXOUT
GND0
GND1
MOD1
MOD0
FIR_EN
AGND
VDD
HSDL_3600#017
C620 0.47uF
C621 6.8uF_16V
Caps must be placed
as close as possible to
pins 1,2
Title
Size A
Project:
Document Number
Rev
Date:
Sheet 33 of 58


SMC Testpoint Header
Boot Mode Programming Straps
P90-P92 needs to be at VCC for boot mode programming. They are already pulled up in the design. MD0, MD1 needs to be at Vss. Jumper for J34 needs to be populated. System needs to supply +V3ALWAYS to flash connector.
SMC/KBC | J35
Enable | 1-2 (Default)
Disable | 2-3
Decode KBC Addresses | J38
Enable 60h & 64h | No Shunt (Default)
Disable | Shunt
Decode SMC Addresses | J37
Enable 62h & 66h | No Shunt (Default)
Disable | Shunt
KBC LED Power Select | J36
+V3S | 1-2 (Default)
+V3A_KBC | 2-3
BLUETOOTH ON/OFF
LID SWITCH
PUSH BUTTON
SW2 SPDT
H8S/2149
Flash Conn
Note: for flash progamming, must use TX1 and RX1, which are pin97 and pin98. Jumper J39 needs to be populated.
GATE OFF PCIRST# during S3
Title
System Management and Keyboard Controller
Size A
Project:
Document Number
Rev
Date:
Sheet 34 of 58


KBC_SCANOUT[15:0] 34
J41
KBC_SCANOUT0
KBC_SCANOUT1
KBC_SCANOUT2
KBC_SCANOUT3
KBC_SCANOUT4
KBC_SCANOUT5
KBC_SCANOUT6
KBC_SCANOUT7
KBC_SCANOUT8
KBC_SCANOUT9
KBC_SCANOUT10
KBC_SCANOUT11
KBC_SCANOUT12
KBC_SCANOUT13
KBC_SCANOUT14
KBC_SCANOUT15
KBC_SCANIN0
KBC_SCANIN1
KBC_SCANIN2
KBC_SCANIN3
KBC_SCANIN4
KBC_SCANIN5
KBC_SCANIN6
KBC_SCANIN7
RIBCAP_CONN
No Stuff
KBC_SCANIN[7:0] 34
12,14,15,16,20,27,29,32,33,40,41,42,43,44,45,46,48 +V5S
CBTD has integrated diode for 5V to 3.3V voltage translation
U39
C629
0.01uF
34 KBC_GP_DATA
34 KBC_GP_CLK
34 KBC_MOUSE_DATA
34 KBC_MOUSE_CLK
34 KBC_KB_DATA
34 KBC_KB_CLK
18 H_A20GATE
GP_DATA
GP_CLK
MOUSE_DATA
MOUSE_CLK
KBD_DATA
KBD_CLK
KBC_A20GATE 34,36
U39_2A3
U39_2A4
U39_2A5
U39_2B3
U39_2B4
U39_2B5
CBTD_3384
R419
4.7K
L27
FER_BEAD_420
GP_CLK
C630
47pF
F2
0.5A
L29
FER_BEAD_50
F3
0.5A
L30
FER_BEAD_50
R420
4.7K
L28
FER_BEAD_420
GP_DATA
C631
47pF
R422
4.7K
L31
FER_BEAD_420
29 KBD_CLK
C635
47pF
L_GPCLK
L_GPDATA
J42
PS2DOUBLE_CONN
R421
4.7K
L32
FER_BEAD_420
KBD_DATA 29
C632
47pF
L33
FER_BEAD_50
If a PS/2 "breakout" connector is used,the keyboard PS/2 connector can be used for both a PS/2 keyboard and a second PS/2 mouse. Otherwise, the keyboard PS/2 connector will only support a PS/2 keyboard.
C633
22uF_20V
C634
0.01uF
R423
4.7K
L35
FER_BEAD_420
29 MOUSE_CLK
C636
47pF
L34
FER_BEAD_50
L36
FER_BEAD_420
R424
4.7K
MOUSE_DATA 29
C637
47pF
Title
Keyboard and Mouse Connectors
Size
A
Project:
Document Number
Rev
Date:
Sheet 35 of 58

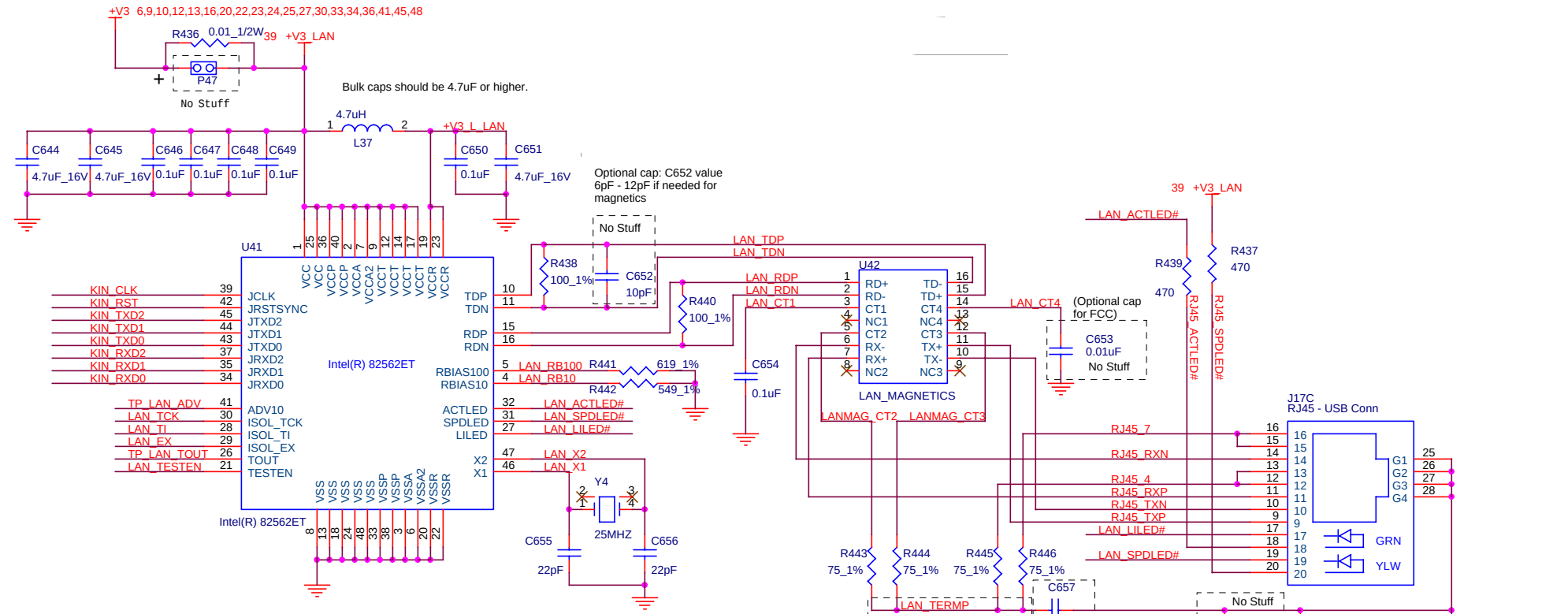

Do Not Stuff
SECURITY
I2C
SMBUS_ICH
For I2C device development work only
I2C Interface is only 3V Tolerant make sure SMC isolates SMB_SC_DATA/CLK!!!
Smart Card Header
J43
J44
LPCSLOT
KEY
J45
HEADER2x15
SMC Sidebands for Power Management
J46
5x2 Header
SIO Sidebands
J47
4x2 Header
TEST HEADER
GROUND HEADERS
MOUNTING HOLES
No Stuff
NO STUFF
SEC_I2C_INT#
SMB_SC_INT#
SMB_ICH_ALRT#
Title
LPC Slot
Size
A
Project:
Document Number
Rev
Date
Sheet 36 of 58





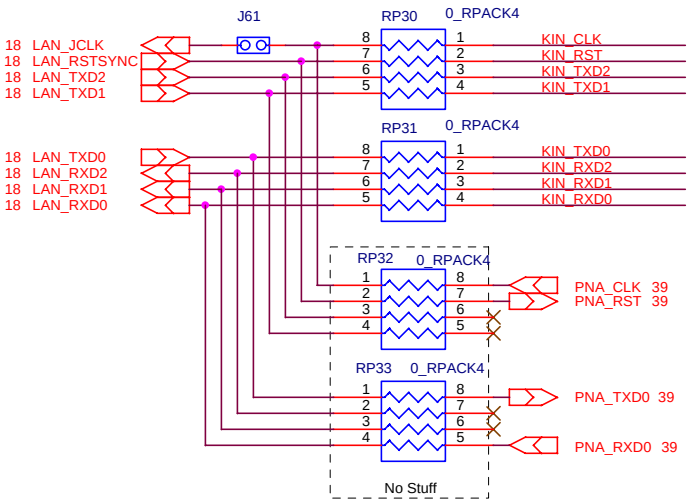
Test point header

Title: LCI / EEPROM			
Size: A	Project:	Document Number	Rev
Date:		Sheet 37 of 58	

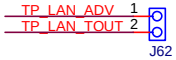


LAN Device Select

Stuff RP30 & RP31 for Kinnereth (RJ-45) [default];
Stuff RP32 & RP33 for Gilad (RJ-11).
Do not stuff both.

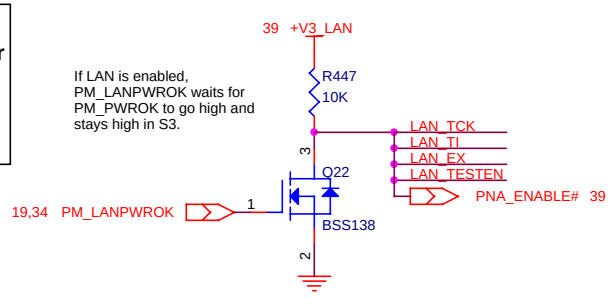


Intel(R) 82562ET Testpoint Header

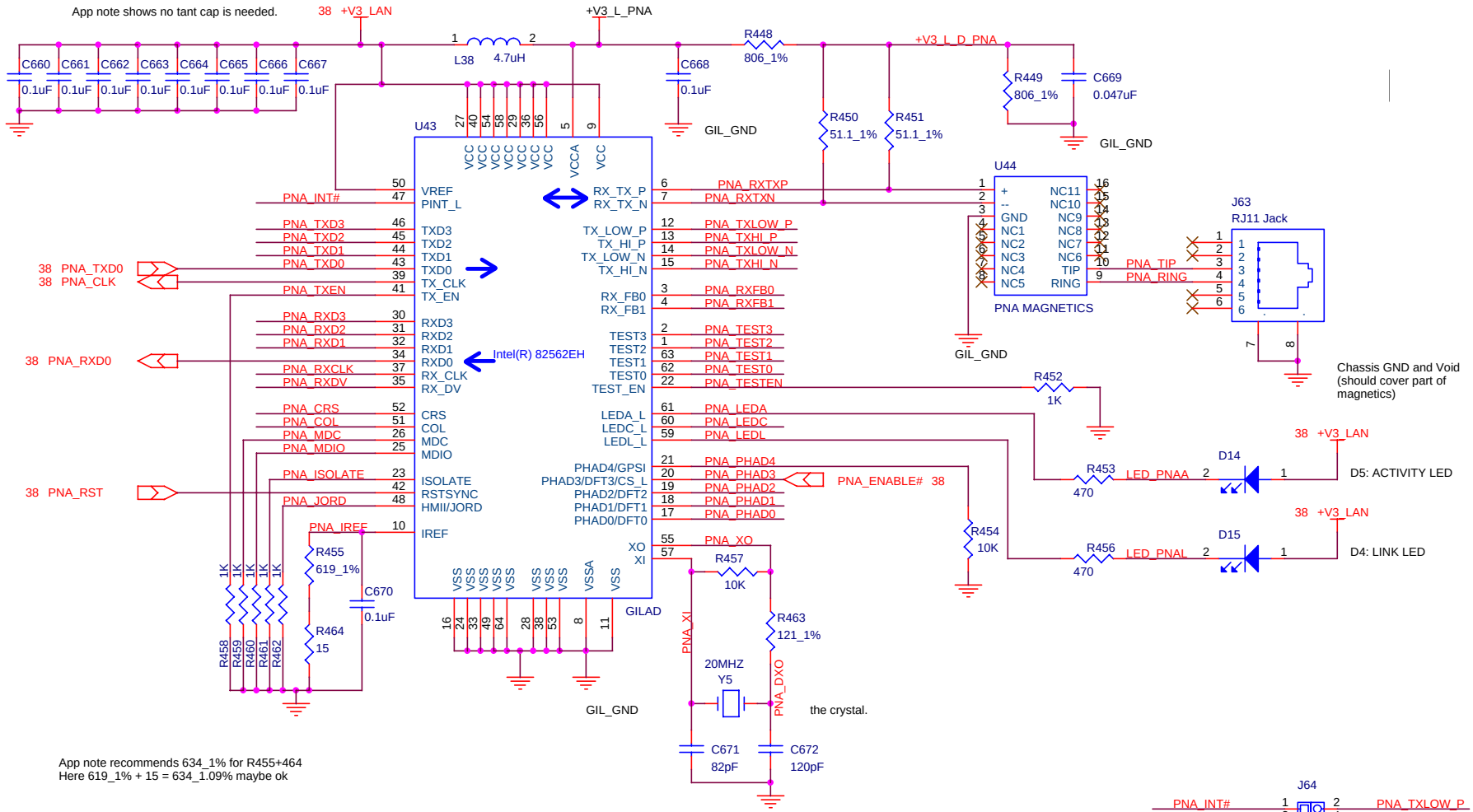


LAN_PHYCLK	J61
Enable	Shunt (Default)
Disable	No Shunt

NOTE: Disable LAN_PHYCLK when not using LAN Interface

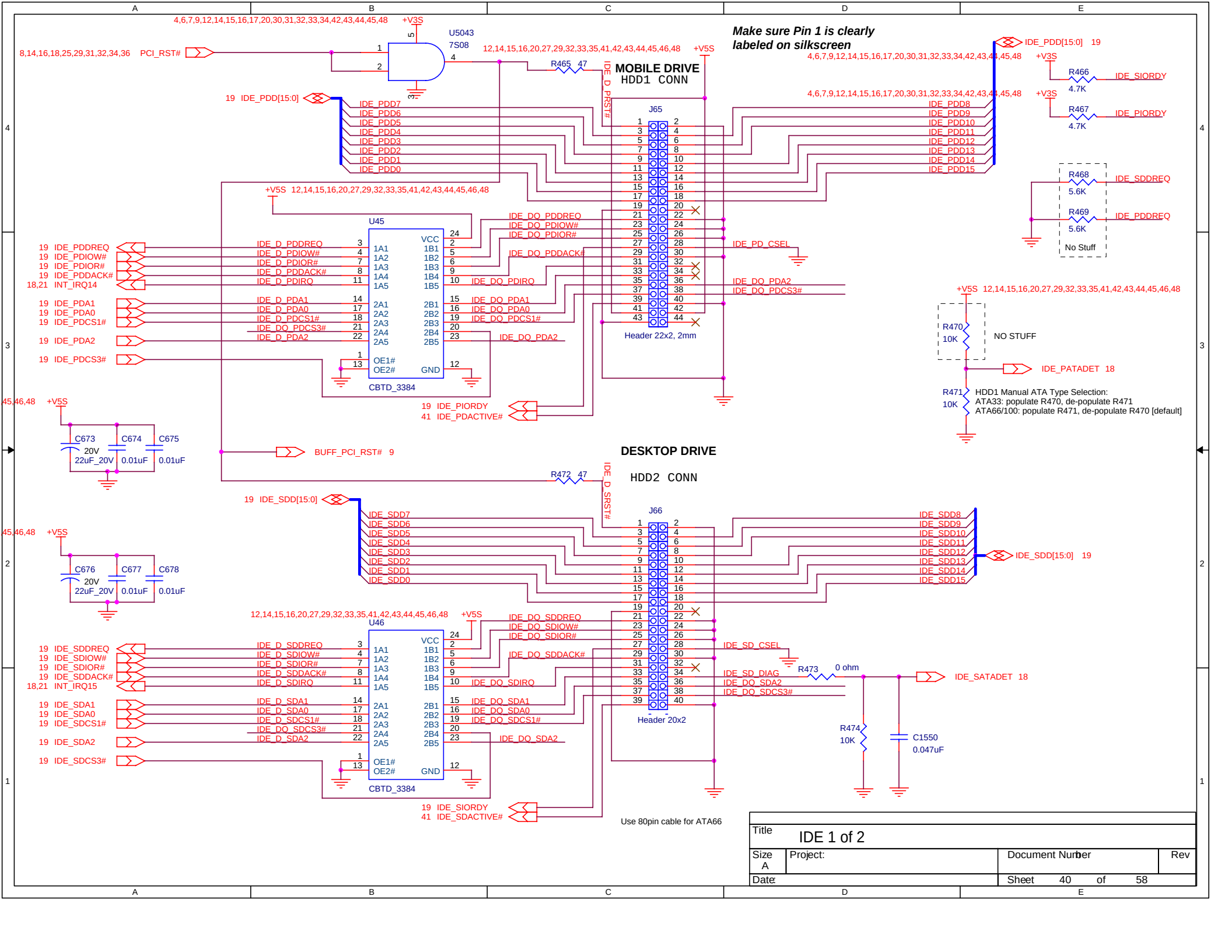


Title	LAN Interface (Intel(R) 82562ET)		
Size A	Project:	Document Number	Rev
Date:		Sheet 38 of 58	

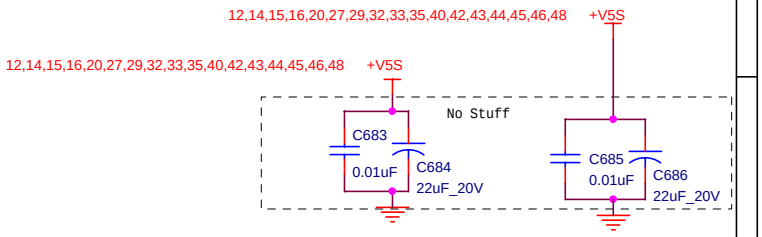


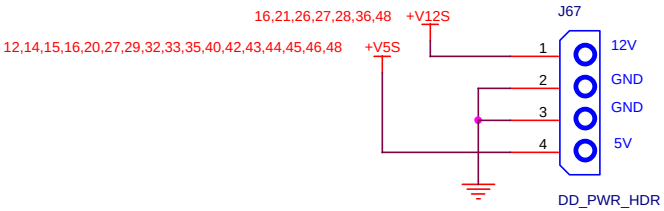
Intel(R) 82562EH Testpoint Header

Title	HomePNA (Intel(R) 82562EH)		
Size A	Project:	Document Number	Rev
Date:		Sheet 39 of 58	

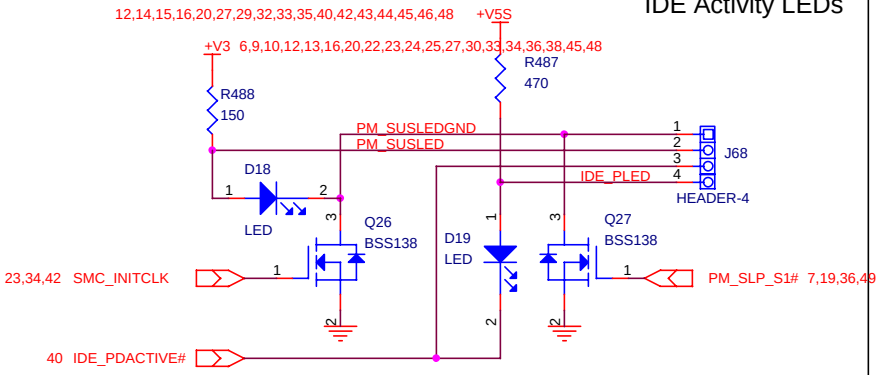

Make sure Pin 1 is clearly labeled on silkscreen
MOBILE DRIVE
HDD1 CONN
DESKTOP DRIVE
HDD2 CONN
U5043
7S08
U45
U46
CBTD_3384
J65
J66
Header 22x2, 2mm
Header 20x2
R465 47
R466 4.7K
R467 4.7K
R468 5.6K
R469 5.6K
No Stuff
R470 10K
NO STUFF
R471 10K
HDD1 Manual ATA Type Selection:
ATA33: populate R470, de-populate R471
ATA66/100: populate R471, de-populate R470 [default]
R472 47
R473 0 ohm
R474 10K
C1550 0.047uF
C673 C674 C675 C676 C677 C678
20V
22uF_20V 0.01uF 0.01uF
Use 80pin cable for ATA66
Title
IDE 1 of 2
Size A
Project:
Document Number
Rev
Date:
Sheet 40 of 58

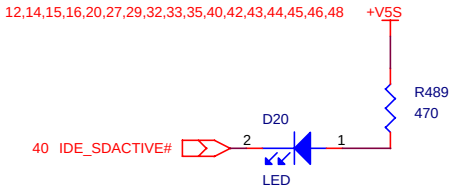
IDE Power Plane Control





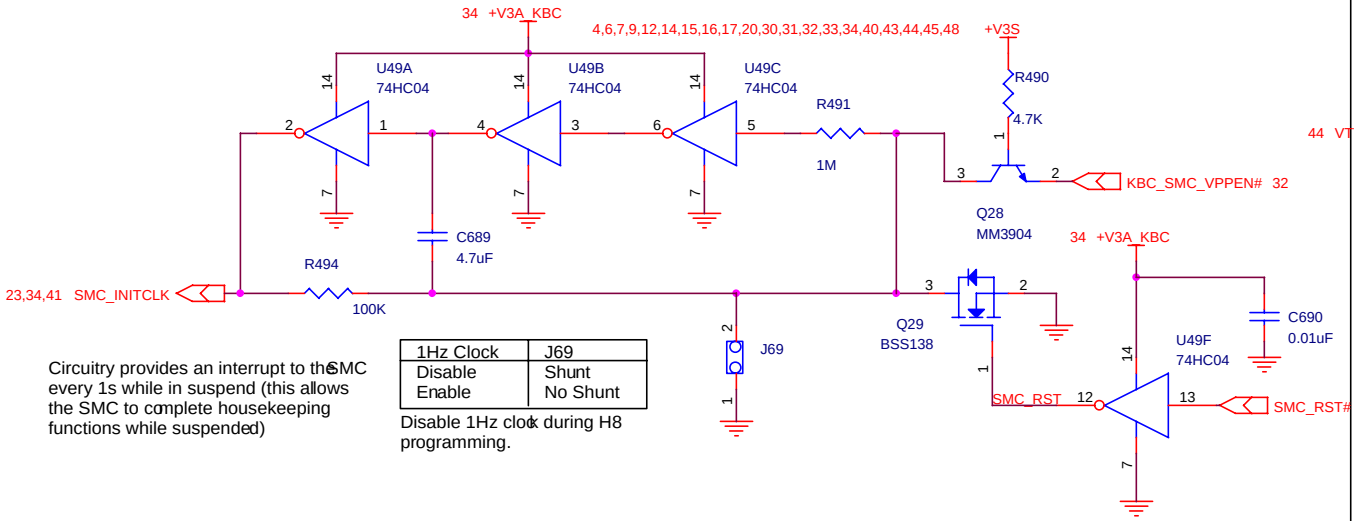
IDE Activity LEDs





Title: IDE 2 of 2			
Size: A	Project:	Document Number	Rev
Date:		Sheet 41 of 58	

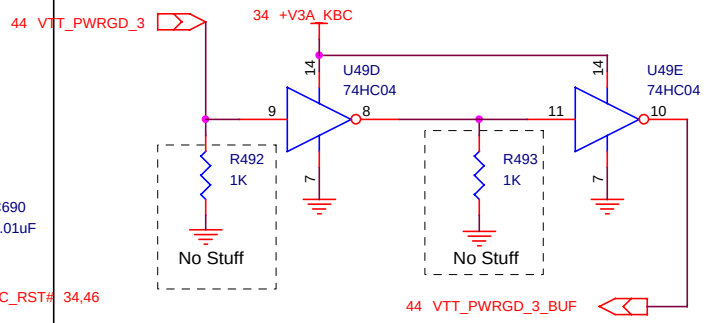
SMC SUSPEND TIMER



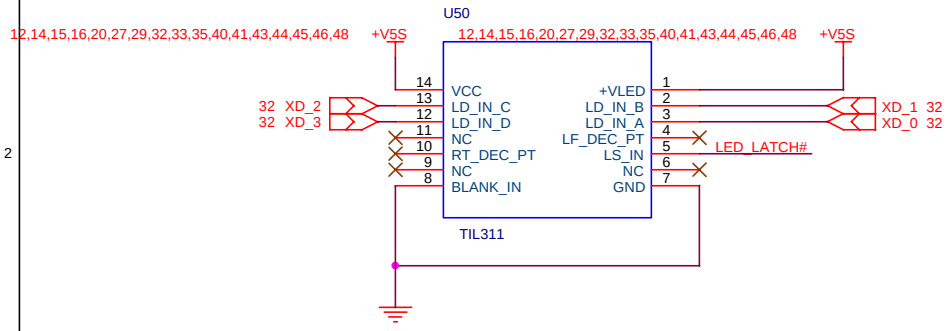
Circuitry provides an interrupt to the SMC every 1s while in suspend (this allows the SMC to complete housekeeping functions while suspended)

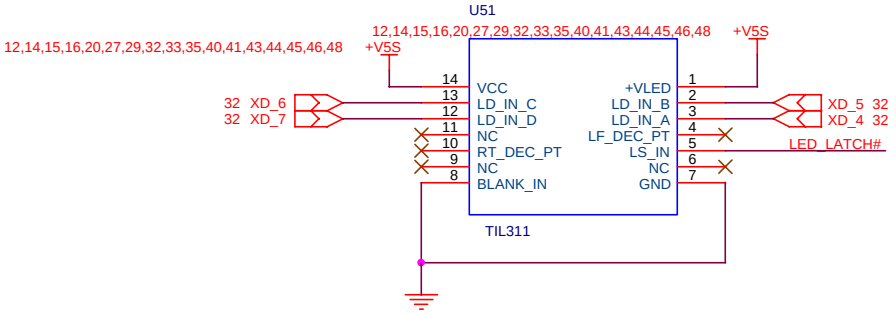
1Hz Clock	J69
Disable	Shunt
Enable	No Shunt

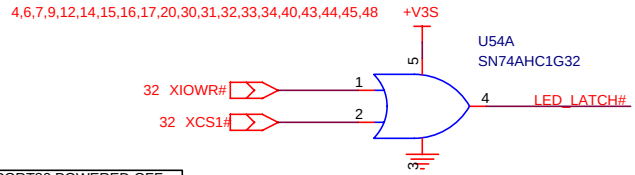
Disable 1Hz clock during H8 programming.



7 SEGMENT DISPLAYS

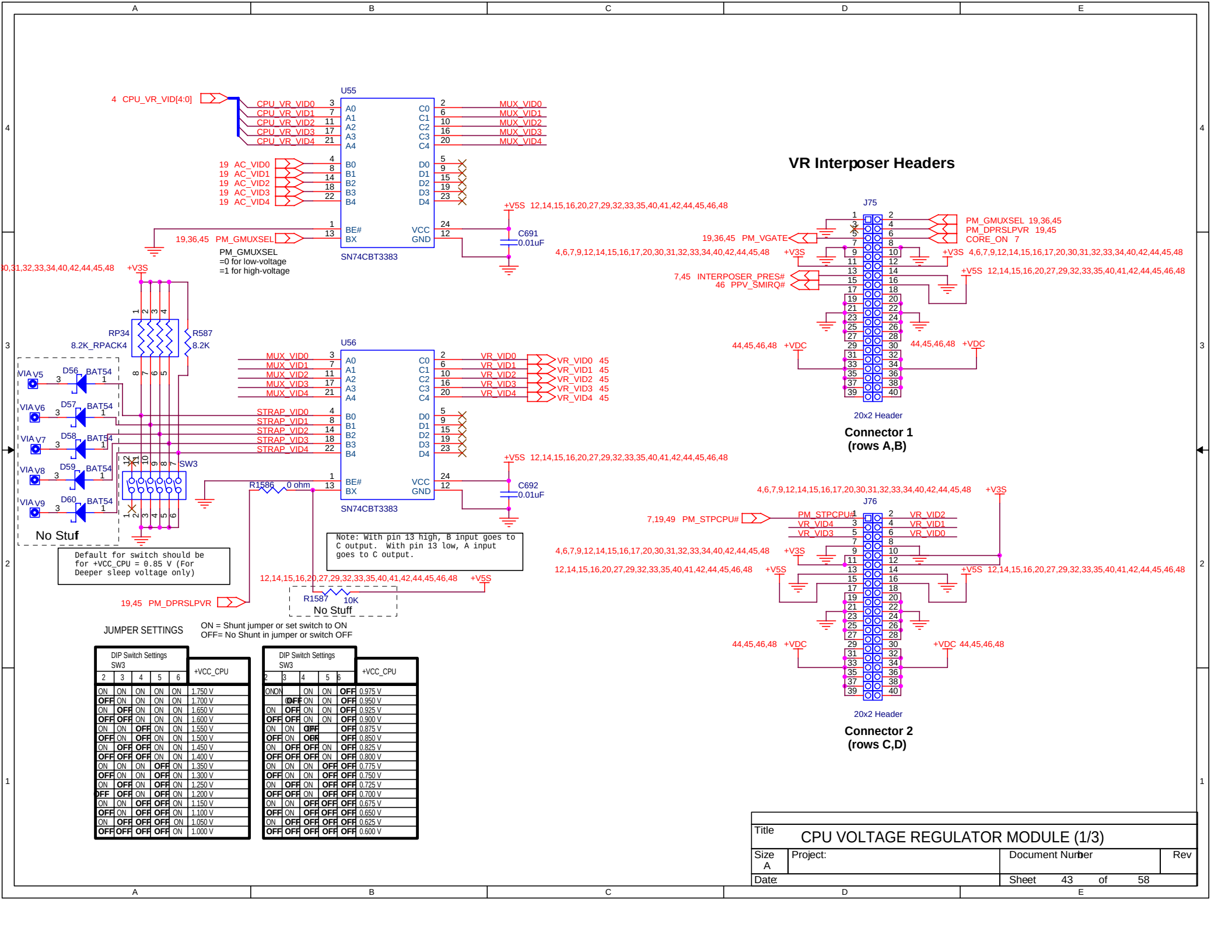






NOTE: PORT80 POWERED OFF DURING STR/STD

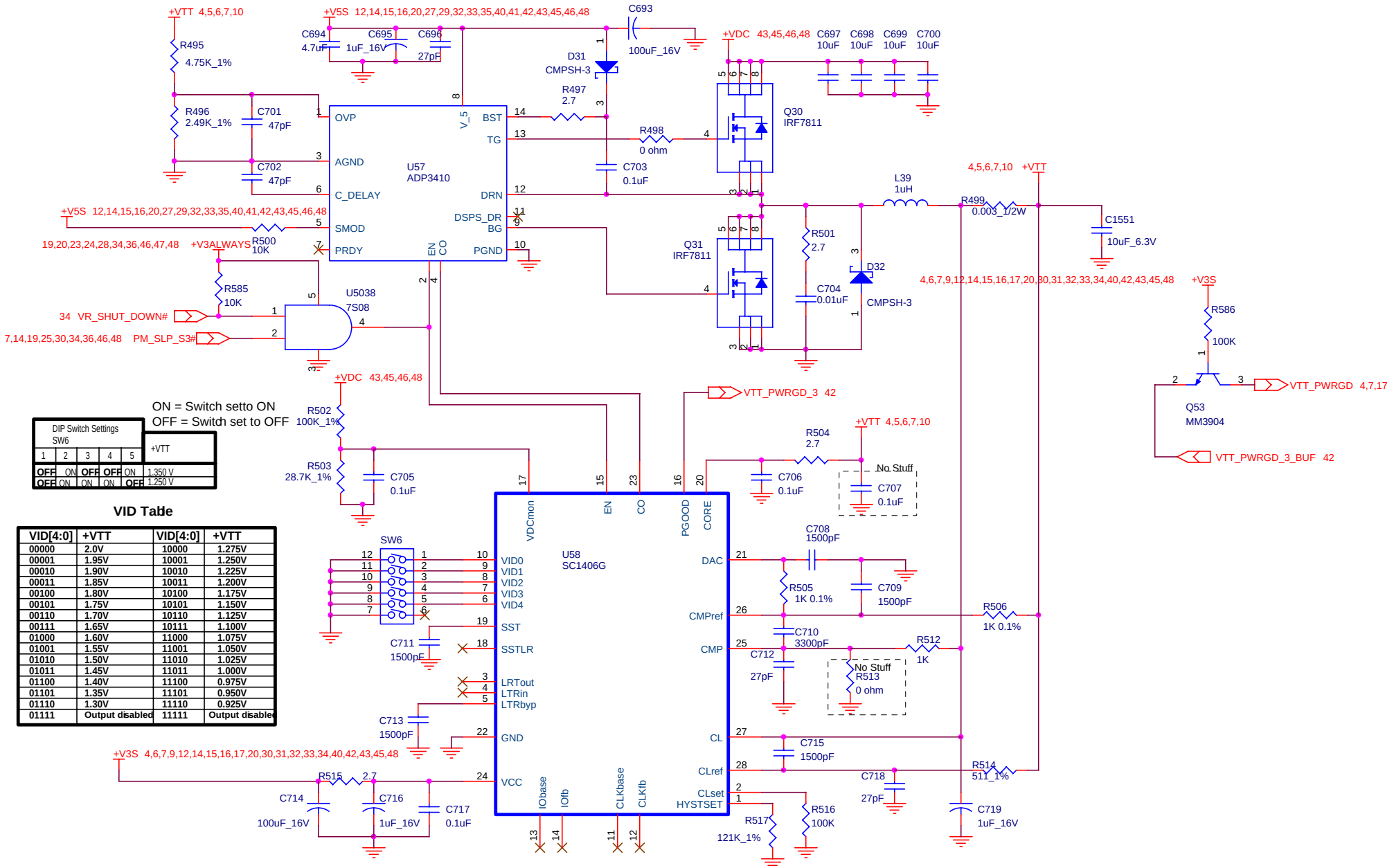
Title: SMC Suspend Timer and Port 80 LEDs			
Size: A	Project:	Document Number	Rev
Date:		Sheet 42 of 58	



DIP Switch Settings SW3					+VCC_CPU
2	3	4	5	6	
ON	ON	ON	ON	ON	1.750 V
OFF	ON	ON	ON	ON	1.700 V
ON	OFF	ON	ON	ON	1.650 V
OFF	OFF	ON	ON	ON	1.600 V
ON	ON	OFF	ON	ON	1.550 V
OFF	ON	OFF	ON	ON	1.500 V
ON	OFF	OFF	ON	ON	1.450 V
OFF	OFF	OFF	ON	ON	1.400 V
ON	ON	ON	OFF	ON	1.350 V
OFF	ON	ON	OFF	ON	1.300 V
ON	OFF	ON	OFF	ON	1.250 V
OFF	OFF	ON	OFF	ON	1.200 V
ON	ON	OFF	OFF	ON	1.150 V
OFF	ON	OFF	OFF	ON	1.100 V
ON	OFF	OFF	OFF	ON	1.050 V
OFF	OFF	OFF	OFF	ON	1.000 V

DIP Switch Settings SW3					+VCC_CPU
2	3	4	5	6	
ON	ON	ON	ON	OFF	0.975 V
ON	OFF	ON	ON	OFF	0.950 V
ON	OFF	ON	ON	OFF	0.925 V
OFF	OFF	ON	ON	OFF	0.900 V
ON	ON	OFF	ON	OFF	0.875 V
OFF	ON	OFF	ON	OFF	0.850 V
ON	OFF	OFF	ON	OFF	0.825 V
OFF	OFF	OFF	ON	OFF	0.800 V
ON	ON	ON	OFF	OFF	0.775 V
OFF	ON	ON	OFF	OFF	0.750 V
ON	OFF	ON	OFF	OFF	0.725 V
OFF	OFF	ON	OFF	OFF	0.700 V
ON	ON	OFF	OFF	OFF	0.675 V
OFF	ON	OFF	OFF	OFF	0.650 V
ON	OFF	OFF	OFF	OFF	0.625 V
OFF	OFF	OFF	OFF	OFF	0.600 V

Title	CPU VOLTAGE REGULATOR MODULE (1/3)		
Size A	Project:	Document Number	Rev
Date:		Sheet 43 of 58	

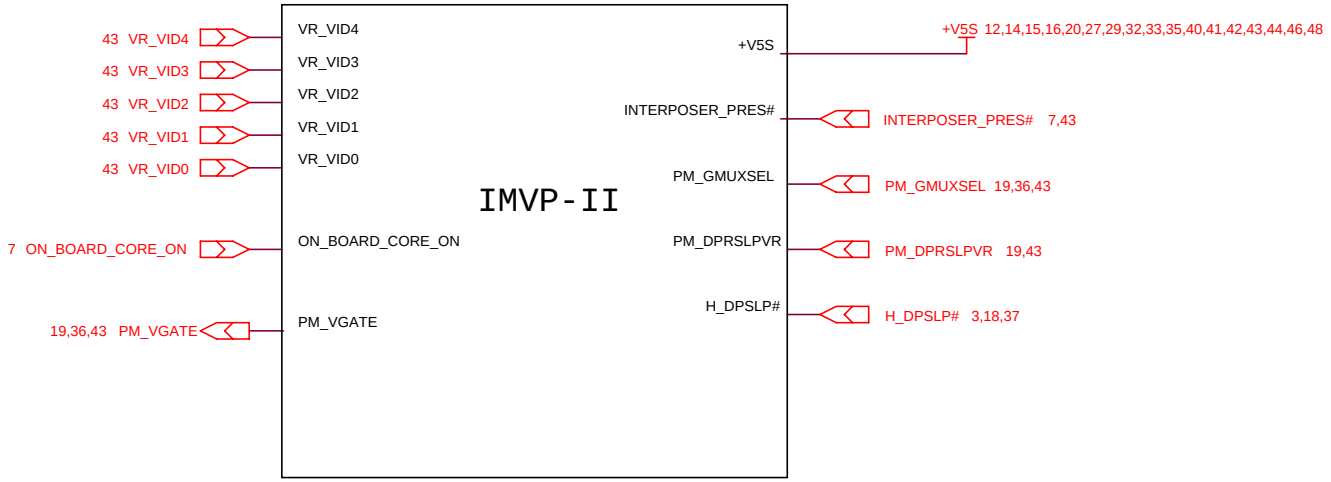


DIP Switch Settings SW6					
1	2	3	4	5	+VTT
OFF	ON	OFF	OFF	ON	1.350 V
OFF	ON	ON	ON	OFF	1.250 V

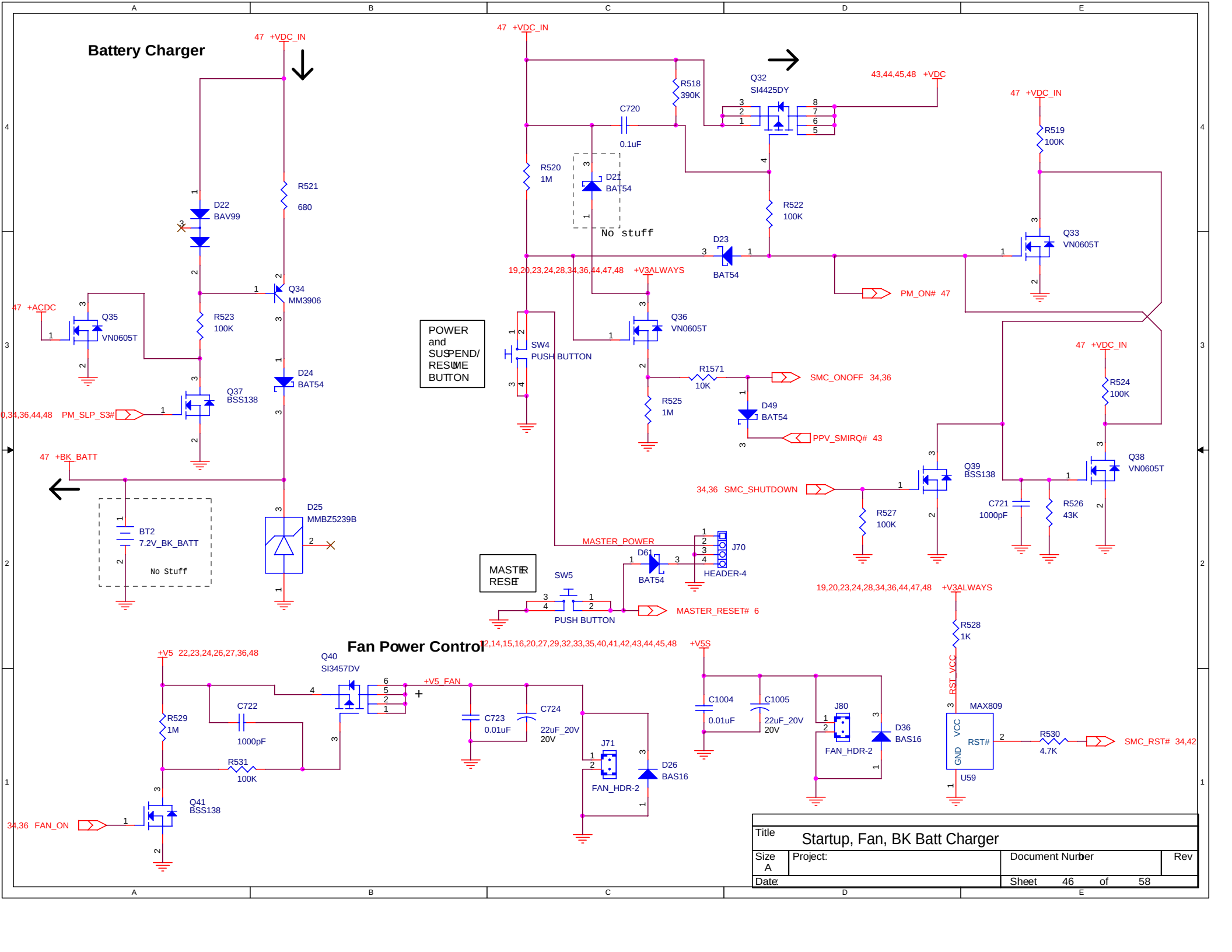
VID Table

VID[4:0]	+VTT	VID[4:0]	+VTT
00000	2.0V	10000	1.275V
00001	1.95V	10001	1.250V
00010	1.90V	10010	1.225V
00011	1.85V	10011	1.200V
00100	1.80V	10100	1.175V
00101	1.75V	10101	1.150V
00110	1.70V	10110	1.125V
00111	1.65V	10111	1.100V
01000	1.60V	11000	1.075V
01001	1.55V	11001	1.050V
01010	1.50V	11010	1.025V
01011	1.45V	11011	1.000V
01100	1.40V	11100	0.975V
01101	1.35V	11101	0.950V
01110	1.30V	11110	0.925V
01111	Output disabled	11111	Output disabled

Title	VRM (VTT) (2/3)		
Size A	Project:	Document Number	Rev
Date: 1		Sheet 44 of 58	



Title: VRM (core) (3/3)			
Size: A	Project:	Document Number	Rev
Date:		Sheet 45 of 58	


Battery Charger
47 +VDC_IN
R521
680
D22
BAV99
R523
100K
Q34
MM3906
47 +ACDC
Q35
VN0605T
Q37
BSS138
0,34,36,44,48 PM_SLP_S3#
47 +BK_BATT
BT2
7.2V_BK_BATT
No Stuff
D24
BAT54
D25
MMBZ5239B
POWER and SUSPEND/ RESUME BUTTON
SW4
PUSH BUTTON
R518
390K
C720
0.1uF
R520
1M
D21
BAT54
No stuff
R522
100K
D23
BAT54
Q32
SI4425DY
43,44,45,48 +VDC
19,20,23,24,28,34,36,44,47,48 +V3ALWAYS
PM_ON# 47
Q36
VN0605T
R1571
10K
SMC_ONOFF 34,36
R525
1M
D49
BAT54
PPV_SMIRQ# 43
R519
100K
Q33
VN0605T
47 +VDC_IN
R524
100K
Q38
VN0605T
Q39
BSS138
34,36 SMC_SHUTDOWN
R527
100K
C721
1000pF
R526
43K
MASTER RESET
MASTER_POWER
D61
BAT54
J70
HEADER-4
SW5
PUSH BUTTON
MASTER_RESET# 6
Fan Power Control
+V5 22,23,24,26,27,36,48
Q40
SI3457DV
+V5_FAN
C722
1000pF
R529
1M
R531
100K
Q41
BSS138
34,36 FAN_ON
C723
0.01uF
C724
22uF_20V
20V
J71
FAN_HDR-2
D26
BAS16
12,14,15,16,20,27,29,32,33,35,40,41,42,43,44,45,48 +V5S
C1004
0.01uF
C1005
22uF_20V
20V
J80
FAN_HDR-2
D36
BAS16
19,20,23,24,28,34,36,44,47,48 +V3ALWAYS
R528
1K
RST_VCC
MAX809
VCC
RST#
GND
U59
R530
4.7K
SMC_RST# 34,42
Title
Startup, Fan, BK Batt Charger
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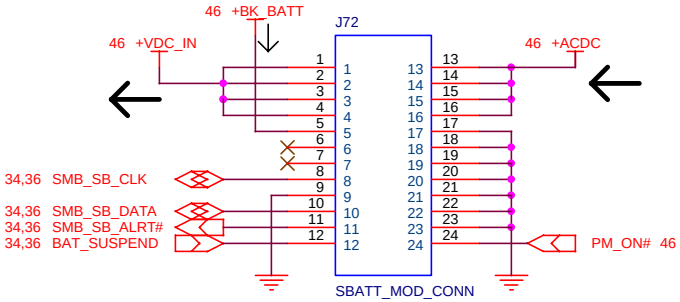
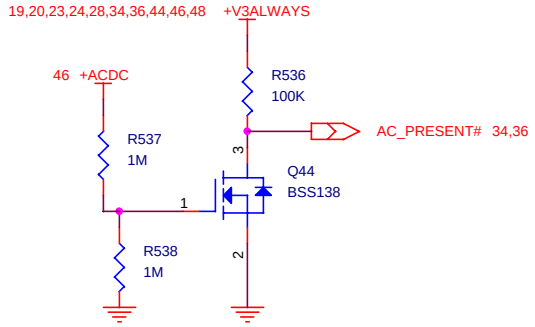
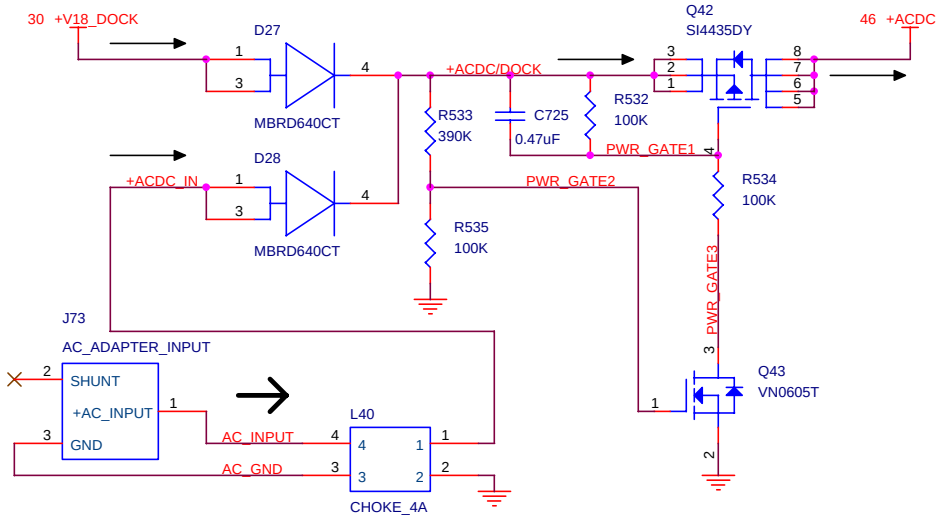
Smart Battery Connector





DC In Selector (Dock or ACDC Jack)



No Stuff

U5005	U5006	U5007	U5008	U5009	U5010	U5011	U5012	U5013	U5014	U5015	U5016	U5017	U5018	U5019	
2mm Shunt	2mm Shunt	2mm Shunt	2mm Shunt	2mm Shunt	2mm Shunt	2mm Shunt	2mm Shunt	2mm Shunt	2mm Shunt	2mm Shunt	2mm Shunt	2mm Shunt	2mm Shunt	2mm Shunt	
U5020	U5021	U5022	U5023	U5024	U5025	U5026	U5027	U5028	U5029	U5030	U5031	U5032	U5033	U5034	
2.54mm Shunt	2.54mm Shunt	2.54mm Shunt	2.54mm Shunt	2.54mm Shunt	2.54mm Shunt	2.54mm Shunt	2.54mm Shunt	2.54mm Shunt	2.54mm Shunt	2.54mm Shunt	2.54mm Shunt	2.54mm Shunt	2.54mm Shunt	2.54mm Shunt	

Title: Smart Batt, AC In			
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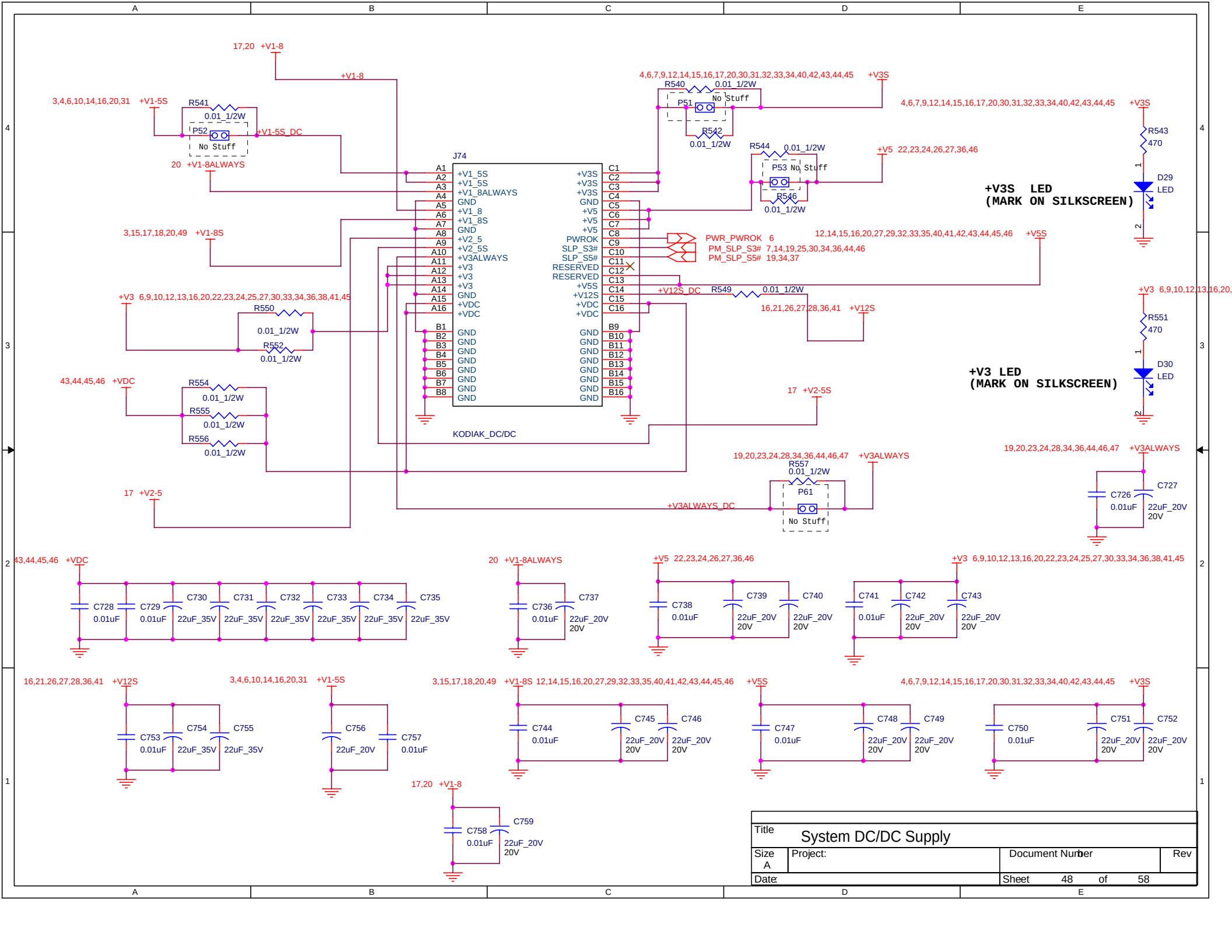
J74
KODIAK_DC/DC
+V3S LED
(MARK ON SILKSCREEN)
+V3 LED
(MARK ON SILKSCREEN)
No Stuff
PWR_PWROK 6
PM_SLP_S3# 7,14,19,25,30,34,36,44,46
PM_SLP_S5# 19,34,37
System DC/DC Supply
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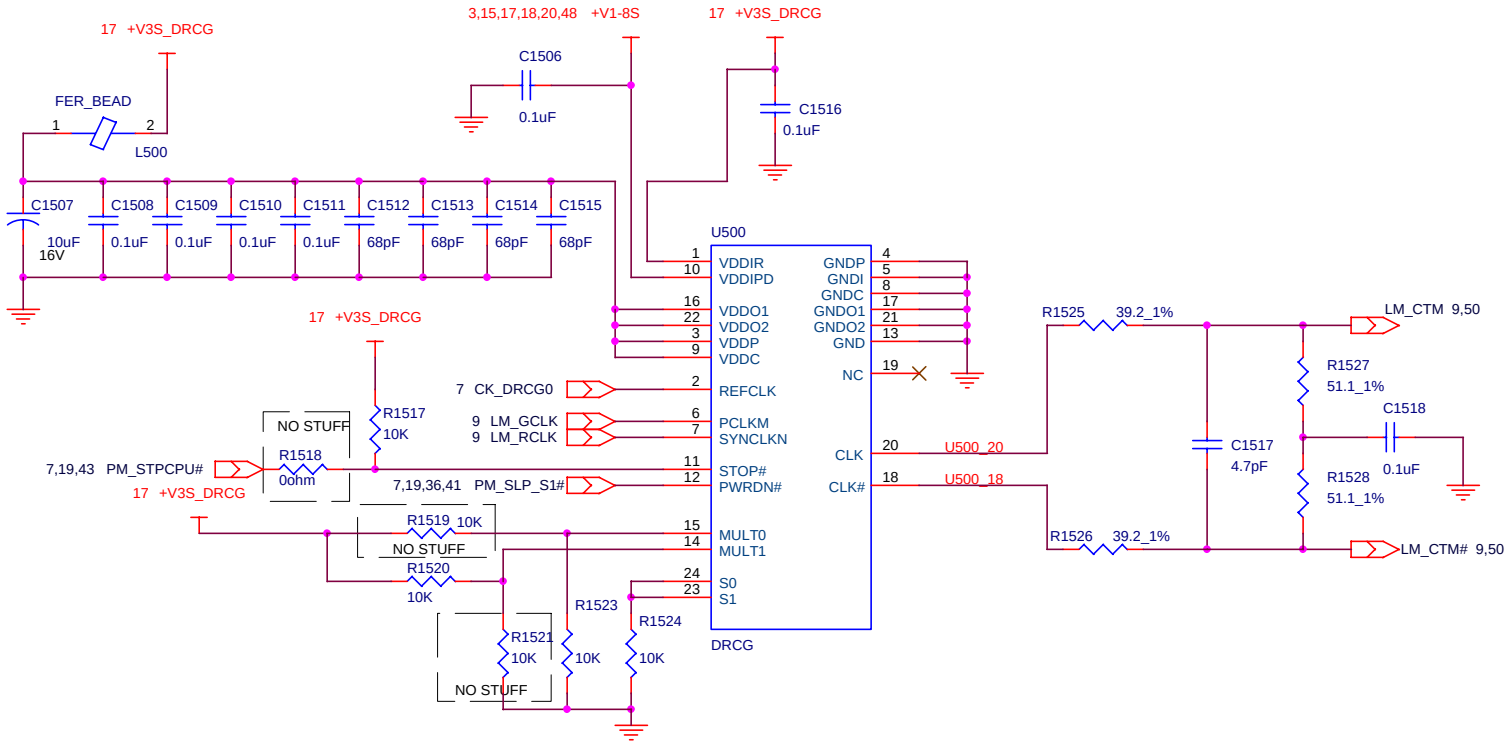

Title: DRCG			
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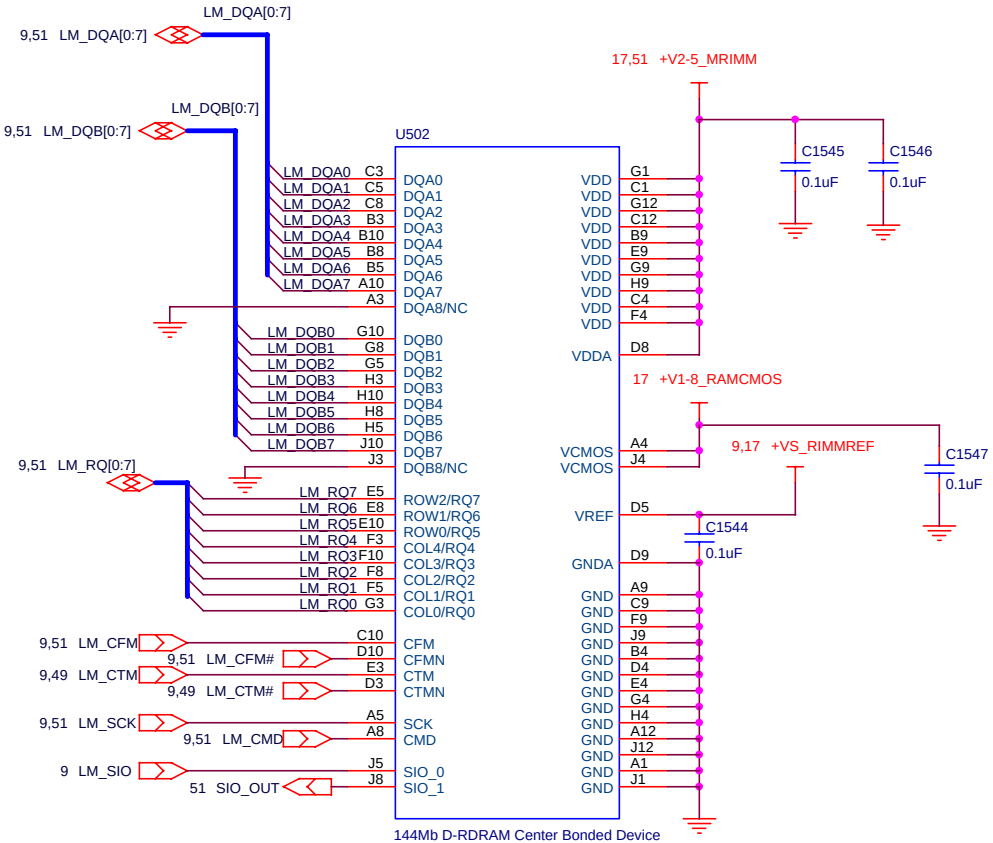

Title: RDRAM DEVICE			
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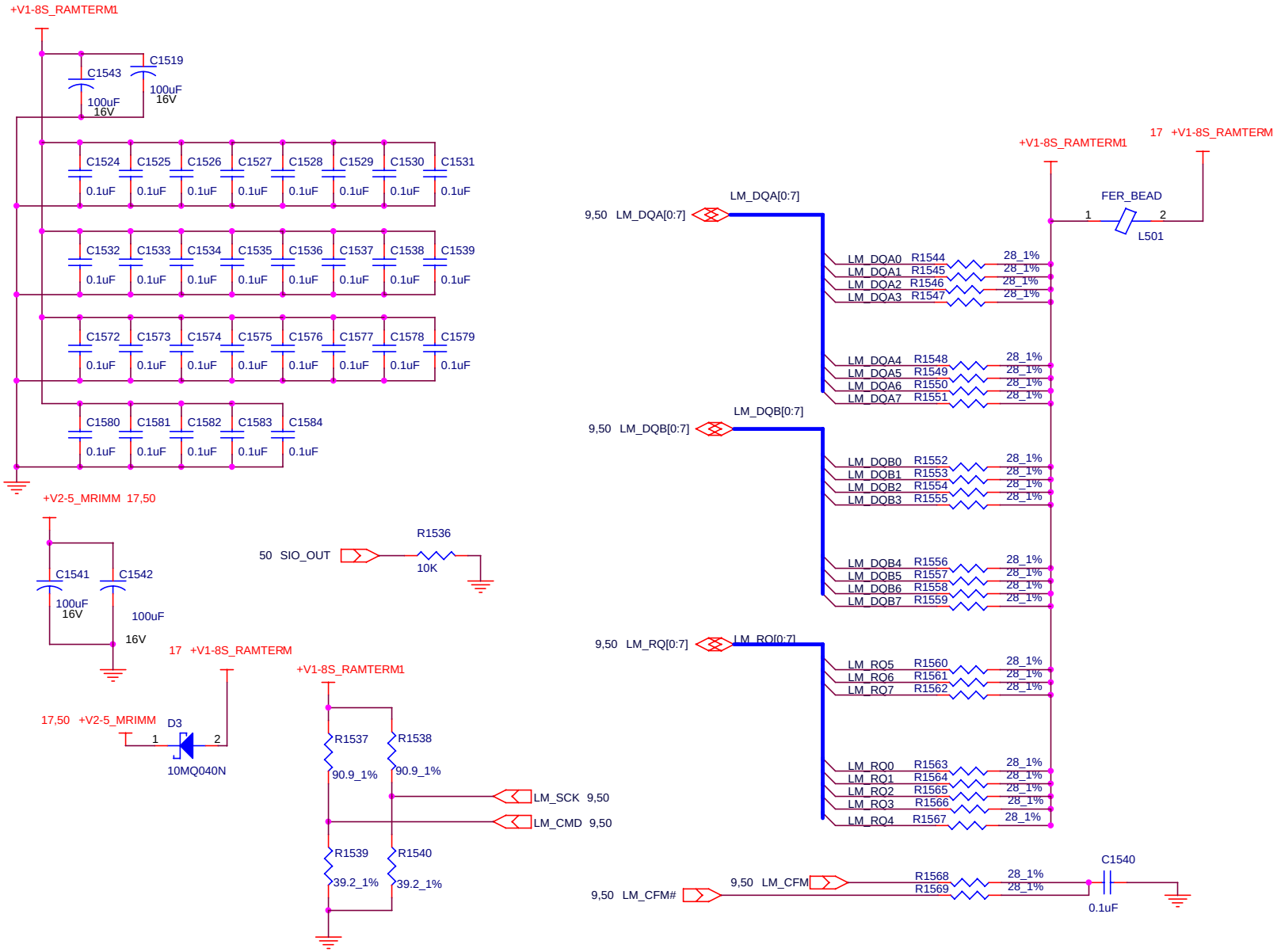

Title	TERMINATIONS & DECOUPLING		
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1	BT1	19	43	C112	5	85	C155	7	127	C197	10	169	C256	10	211	C301	13	253	C343	13
2	BT2	46	44	C113	5	86	C156	8	128	C198	10	170	C257	10	212	C302	13	254	C344	13
3	C1	3	45	C114	5	87	C157	8	129	C199	10	171	C258	10	213	C303	13	255	C345	13
4	C2	4	46	C115	5	88	C158	8	130	C200	10	172	C259	10	214	C304	13	256	C346	13
5	C3	4	47	C116	5	89	C159	8	131	C201	10	173	C260	10	215	C305	13	257	C347	13
6	C4	4	48	C117	5	90	C160	9	132	C202	10	174	C261	10	216	C306	13	258	C348	13
7	C5	4	49	C118	5	91	C161	9	133	C205	10	175	C262	10	217	C307	13	259	C350	13
8	C6	4	50	C119	5	92	C162	10	134	C206	10	176	C263	10	218	C308	13	260	C352	14
9	C7	4	51	C120	5	93	C163	10	135	C207	10	177	C264	10	219	C309	13	261	C353	14
10	C20	5	52	C121	6	94	C164	10	136	C208	10	178	C265	10	220	C310	13	262	C355	14
11	C21	5	53	C122	6	95	C165	10	137	C209	10	179	C266	10	221	C311	13	263	C356	14
12	C22	5	54	C123	7	96	C166	10	138	C210	10	180	C267	10	222	C312	13	264	C357	14
13	C23	5	55	C124	7	97	C167	10	139	C211	10	181	C268	10	223	C313	13	265	C358	14
14	C24	5	56	C125	7	98	C168	10	140	C212	10	182	C269	10	224	C314	13	266	C359	14
15	C25	5	57	C126	7	99	C169	10	141	C213	10	183	C270	10	225	C315	13	267	C360	14
16	C26	5	58	C127	7	100	C170	10	142	C214	10	184	C271	10	226	C316	13	268	C361	14
17	C27	5	59	C128	7	101	C171	10	143	C215	10	185	C272	10	227	C317	13	269	C362	14
18	C28	5	60	C129	7	102	C172	10	144	C226	10	186	C273	10	228	C318	13	270	C363	14
19	C29	5	61	C130	7	103	C173	10	145	C227	10	187	C274	10	229	C319	13	271	C364	14
20	C30	5	62	C131	7	104	C174	10	146	C228	10	188	C275	10	230	C320	13	272	C365	14
21	C31	5	63	C132	7	105	C175	10	147	C229	10	189	C276	10	231	C321	13	273	C366	15
22	C32	5	64	C133	7	106	C176	10	148	C230	10	190	C277	10	232	C322	13	274	C367	15
23	C33	5	65	C134	7	107	C177	10	149	C231	10	191	C278	10	233	C323	13	275	C368	15
24	C34	5	66	C135	7	108	C178	10	150	C233	10	192	C279	10	234	C324	13	276	C369	15
25	C35	5	67	C136	7	109	C179	10	151	C234	10	193	C280	10	235	C325	13	277	C370	15
26	C36	5	68	C137	7	110	C180	10	152	C239	10	194	C281	10	236	C326	13	278	C371	15
27	C41	5	69	C138	7	111	C181	10	153	C240	10	195	C282	10	237	C327	13	279	C372	15
28	C42	5	70	C139	7	112	C182	10	154	C241	10	196	C283	10	238	C328	13	280	C373	15
29	C43	5	71	C141	7	113	C183	9	155	C242	10	197	C284	10	239	C329	13	281	C374	15
30	C44	5	72	C142	7	114	C184	10	156	C243	10	198	C285	10	240	C330	13	282	C375	15
31	C55	5	73	C143	7	115	C185	10	157	C244	10	199	C289	13	241	C331	13	283	C376	15
32	C56	5	74	C144	7	116	C186	10	158	C245	10	200	C290	13	242	C332	13	284	C377	15
33	C57	5	75	C145	7	117	C187	10	159	C246	10	201	C291	13	243	C333	13	285	C378	15
34	C58	5	76	C146	7	118	C188	10	160	C247	10	202	C292	13	244	C334	13	286	C379	15
35	C59	5	77	C147	7	119	C189	10	161	C248	10	203	C293	13	245	C335	13	287	C380	15
36	C60	5	78	C148	7	120	C190	10	162	C249	10	204	C294	13	246	C336	13	288	C381	16
37	C61	5	79	C149	7	121	C191	10	163	C250	10	205	C295	13	247	C337	13	289	C382	16
38	C72	5	80	C150	7	122	C192	10	164	C251	10	206	C296	13	248	C338	13	290	C383	16
39	C73	5	81	C151	7	123	C193	10	165	C252	10	207	C297	13	249	C339	13	291	C384	16
40	C74	5	82	C152	7	124	C194	10	166	C253	10	208	C298	13	250	C340	13	292	C385	16
41	C75	5	83	C153	7	125	C195	10	167	C254	10	209	C299	13	251	C341	13	293	C386	16
42	C111	5	84	C154	7	126	C196	10	168	C255	10	210	C300	13	252	C342	13	294	C387	16

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295	C388	16	337	C437	20	379	C479	20	421	C521	26	463	C563	27	505	C605	32	547	C647	38
296	C389	16	338	C438	20	380	C480	22	422	C522	26	464	C564	27	506	C606	32	548	C648	38
297	C390	16	339	C439	20	381	C481	22	423	C523	26	465	C565	27	507	C607	32	549	C649	38
298	C391	16	340	C440	20	382	C482	22	424	C524	26	466	C566	27	508	C608	32	550	C650	38
299	C392	16	341	C441	20	383	C483	22	425	C525	26	467	C567	27	509	C609	32	551	C651	38
300	C393	16	342	C442	20	384	C484	22	426	C526	26	468	C568	27	510	C610	32	552	C652	38
301	C394	16	343	C443	20	385	C485	23	427	C527	26	469	C569	27	511	C611	33	553	C653	38
302	C395	16	344	C444	20	386	C486	23	428	C528	26	470	C570	27	512	C612	33	554	C654	38
303	C396	16	345	C445	20	387	C487	23	429	C529	26	471	C571	27	513	C613	33	555	C655	38
304	C397	16	346	C446	20	388	C488	23	430	C530	26	472	C572	27	514	C614	33	556	C656	38
305	C398	16	347	C447	20	389	C489	23	431	C531	26	473	C573	27	515	C615	33	557	C657	38
306	C399	16	348	C448	20	390	C490	23	432	C532	26	474	C574	27	516	C616	33	558	C658	38
307	C400	16	349	C449	20	391	C491	23	433	C533	26	475	C575	27	517	C617	33	559	C659	38
308	C401	16	350	C450	20	392	C492	24	434	C534	26	476	C576	27	518	C618	33	560	C660	39
309	C402	16	351	C451	20	393	C493	24	435	C535	26	477	C577	27	519	C619	33	561	C661	39
310	C403	16	352	C452	20	394	C494	24	436	C536	26	478	C578	27	520	C620	33	562	C662	39
311	C404	16	353	C453	20	395	C495	24	437	C537	26	479	C579	28	521	C621	33	563	C663	39
312	C405	16	354	C454	20	396	C496	24	438	C538	26	480	C580	28	522	C622	34	564	C664	39
313	C406	16	355	C455	20	397	C497	25	439	C539	26	481	C581	28	523	C623	34	565	C665	39
314	C407	16	356	C456	20	398	C498	25	440	C540	27	482	C582	28	524	C624	34	566	C666	39
315	C408	16	357	C457	20	399	C499	25	441	C541	27	483	C583	29	525	C625	34	567	C667	39
316	C409	16	358	C458	20	400	C500	25	442	C542	27	484	C584	29	526	C626	34	568	C668	39
317	C410	16	359	C459	20	401	C501	25	443	C543	27	485	C585	29	527	C627	34	569	C669	39
318	C411	16	360	C460	20	402	C502	25	444	C544	27	486	C586	29	528	C628	34	570	C670	39
319	C412	16	361	C461	20	403	C503	25	445	C545	27	487	C587	29	529	C629	35	571	C671	39
320	C420	18	362	C462	20	404	C504	25	446	C546	27	488	C588	29	530	C630	35	572	C672	39
321	C421	18	363	C463	20	405	C505	25	447	C547	27	489	C589	29	531	C631	35	573	C673	40
322	C422	18	364	C464	20	406	C506	25	448	C548	27	490	C590	30	532	C632	35	574	C674	40
323	C423	18	365	C465	20	407	C507	25	449	C549	27	491	C591	31	533	C633	35	575	C675	40
324	C424	19	366	C466	20	408	C508	25	450	C550	27	492	C592	31	534	C634	35	576	C676	40
325	C425	19	367	C467	20	409	C509	25	451	C551	27	493	C593	31	535	C635	35	577	C677	40
326	C426	19	368	C468	20	410	C510	25	452	C552	27	494	C594	31	536	C636	35	578	C678	40
327	C427	19	369	C469	20	411	C511	25	453	C553	27	495	C595	31	537	C637	35	579	C683	41
328	C428	19	370	C470	20	412	C512	25	454	C554	27	496	C596	32	538	C638	36	580	C684	41
329	C429	20	371	C471	20	413	C513	25	455	C555	27	497	C597	32	539	C639	36	581	C685	41
330	C430	20	372	C472	20	414	C514	25	456	C556	27	498	C598	32	540	C640	36	582	C686	41
331	C431	20	373	C473	20	415	C515	25	457	C557	27	499	C599	32	541	C641	36	583	C689	42
332	C432	20	374	C474	20	416	C516	25	458	C558	27	500	C600	32	542	C642	36	584	C690	42
333	C433	20	375	C475	20	417	C517	25	459	C559	27	501	C601	32	543	C643	36	585	C691	43
334	C434	20	376	C476	20	418	C518	25	460	C560	27	502	C602	32	544	C644	38	586	C692	43
335	C435	20	377	C477	20	419	C519	26	461	C561	27	503	C603	32	545	C645	38	587	C693	44
336	C436	20	378	C478	20	420	C520	26	462	C562	27	504	C604	32	546	C646	38	588	C694	44

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589	C695	44	631	C737	48	673	C781	24	715	C823	5	757	C1537	51	799	C1580	51	841	D40	22
590	C696	44	632	C738	48	674	C782	24	716	C824	5	758	C1538	51	800	C1581	51	842	D41	23
591	C697	44	633	C739	48	675	C783	5	717	C825	5	759	C1539	51	801	C1582	51	843	D42	23
592	C698	44	634	C740	48	676	C784	5	718	C826	5	760	C1540	51	802	C1583	51	844	D43	23
593	C699	44	635	C741	48	677	C785	5	719	C827	5	761	C1541	51	803	C1584	51	845	D44	23
594	C700	44	636	C742	48	678	C786	5	720	C828	5	762	C1542	51	804	D1	15	846	D45	23
595	C701	44	637	C743	48	679	C787	45	721	C829	5	763	C1543	51	805	D2	15	847	D46	23
596	C702	44	638	C744	48	680	C788	45	722	C830	5	764	C1544	50	806	D3	51	848	D47	23
597	C703	44	639	C745	48	681	C789	45	723	C831	5	765	C1545	50	807	D4	19	849	D48	23
598	C704	44	640	C746	48	682	C790	45	724	C1000	15	766	C1546	50	808	D5	19	850	D49	46
599	C705	44	641	C747	48	683	C791	45	725	C1001	10	767	C1547	50	809	D6	20	851	D50	7
600	C706	44	642	C748	48	684	C792	45	726	C1002	10	768	C1548	7	810	D7	23	852	D51	7
601	C707	44	643	C749	48	685	C793	45	727	C1003	10	769	C1549	7	811	D8	25	853	D52	32
602	C708	44	644	C750	48	686	C794	45	728	C1004	46	770	C1550	40	812	D9	30	854	D53	32
603	C709	44	645	C751	48	687	C795	45	729	C1005	46	771	C1551	44	813	D10	32	855	D54	32
604	C710	44	646	C752	48	688	C796	45	730	C1506	49	772	C1552	45	814	D11	34	856	D55	32
605	C711	44	647	C753	48	689	C797	45	731	C1507	49	773	C1553	45	815	D12	34	857	D56	43
606	C712	44	648	C754	48	690	C798	45	732	C1508	49	774	C1554	7	816	D13	34	858	D57	43
607	C713	44	649	C755	48	691	C799	45	733	C1509	49	775	C1555	17	817	D14	39	859	D58	43
608	C714	44	650	C756	48	692	C800	5	734	C1510	49	776	C1556	8	818	D15	39	860	D59	43
609	C715	44	651	C757	48	693	C801	12	735	C1511	49	777	C1557	8	819	D18	41	861	D60	43
610	C716	44	652	C758	48	694	C802	10	736	C1512	49	778	C1559	8	820	D19	41	862	D61	46
611	C717	44	653	C759	48	695	C803	10	737	C1513	49	779	C1560	22	821	D20	41	863	F1	15
612	C718	44	654	C760	5	696	C804	10	738	C1514	49	780	C1561	22	822	D21	46	864	F2	35
613	C719	44	655	C762	7	697	C805	17	739	C1515	49	781	C1562	22	823	D22	46	865	F3	35
614	C720	46	656	C764	10	698	C806	17	740	C1516	49	782	C1563	22	824	D23	46	866	GND1	36
615	C721	46	657	C765	10	699	C807	17	741	C1517	49	783	C1564	23	825	D24	46	867	GND2	36
616	C722	46	658	C766	10	700	C808	5	742	C1518	49	784	C1565	23	826	D25	46	868	GND3	36
617	C723	46	659	C767	10	701	C809	5	743	C1519	51	785	C1566	23	827	D26	46	869	GND4	36
618	C724	46	660	C768	10	702	C810	5	744	C1524	51	786	C1567	23	828	D27	47	870	GND5	36
619	C725	47	661	C769	20	703	C811	5	745	C1525	51	787	C1568	23	829	D28	47	871	GND6	36
620	C726	48	662	C770	20	704	C812	5	746	C1526	51	788	C1569	23	830	D29	48	872	GND7	36
621	C727	48	663	C771	20	705	C813	5	747	C1527	51	789	C1570	23	831	D30	48	873	GND8	36
622	C728	48	664	C772	10	706	C814	5	748	C1528	51	790	C1571	23	832	D31	44	874	GND9	36
623	C729	48	665	C773	10	707	C815	5	749	C1529	51	791	C1572	51	833	D32	44	875	GND10	36
624	C730	48	666	C774	10	708	C816	5	750	C1530	51	792	C1573	51	834	D33	30	876	GND11	36
625	C731	48	667	C775	10	709	C817	5	751	C1531	51	793	C1574	51	835	D34	45	877	GND12	36
626	C732	48	668	C776	20	710	C818	5	752	C1532	51	794	C1575	51	836	D35	45	878	GND13	36
627	C733	48	669	C777	24	711	C819	5	753	C1533	51	795	C1576	51	837	D36	46	879	GND14	36
628	C734	48	670	C778	24	712	C820	5	754	C1534	51	796	C1577	51	838	D37	22	880	GND15	36
629	C735	48	671	C779	24	713	C821	5	755	C1535	51	797	C1578	51	839	D38	22	881	JP1	7
630	C736	48	672	C780	24	714	C822	5	756	C1536	51	798	C1579	51	840	D39	22	882	JP2	14

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885	JP6	32	927	J36	34	969	L7	15	1011	L505	22	1053	P28	20	1095	Q19	34	1137	RP24	21
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887	J4	11	929	J38	34	971	L9	15	1013	L507	23	1055	P30	20	1097	Q21	34	1139	RP26	32
888	J5	12	930	J39	34	972	L10	15	1014	L508	23	1056	P31	22	1098	Q22	38	1140	RP27	32
889	J6	14	931	J40	34	973	L11	22	1015	L509	23	1057	P32	23	1099	Q26	41	1141	RP28	32
890	J7A	33	932	J41	35	974	L14	22	1016	L510	23	1058	P33	23	1100	Q27	41	1142	RP29	32
891	J7B	33	933	J42	35	975	L15	22	1017	L511	23	1059	P34	24	1101	Q28	42	1143	RP30	38
892	J7C	15	934	J43	36	976	L18	22	1018	L512	23	1060	P35	24	1102	Q29	42	1144	RP31	38
893	J8	16	935	J44	36	977	L19	23	1019	L513	23	1061	P36	24	1103	Q30	44	1145	RP32	38
894	J9	16	936	J45	36	978	L22	23	1020	L514	23	1062	P37	25	1104	Q31	44	1146	RP33	38
895	J10	18	937	J46	36	979	L23	23	1021	M1	36	1063	P38	26	1105	Q32	46	1147	RP34	43
896	J11	19	938	J47	36	980	L26	23	1022	M2	36	1064	P39	27	1106	Q33	46	1148	RP35	12
897	J12	21	939	J61	38	981	L27	35	1023	M3	36	1065	P40	27	1107	Q34	46	1149	RP36	12
898	J13	21	940	J62	38	982	L28	35	1024	M4	36	1066	P41	31	1108	Q35	46	1150	RP37	12
899	J14	21	941	J63	39	983	L29	35	1025	M6	36	1067	P42	32	1109	Q36	46	1151	R1	3
900	J15	21	942	J64	39	984	L30	35	1026	M8	36	1068	P43	33	1110	Q37	46	1152	R2	3
901	J16A	22	943	J65	40	985	L31	35	1027	M10	36	1069	P44	34	1111	Q38	46	1153	R3	3
902	J16B	22	944	J66	40	986	L32	35	1028	M11	36	1070	P45	36	1112	Q39	46	1154	R4	3
903	J17A	23	945	J67	41	987	L33	35	1029	M12	36	1071	P46	36	1113	Q40	46	1155	R5	3
904	J17B	23	946	J68	41	988	L34	35	1030	P1	5	1072	P47	38	1114	Q41	46	1156	R6	3
905	J17C	38	947	J69	42	989	L35	35	1031	P2	45	1073	P51	48	1115	Q42	47	1157	R7	3
906	J18	23	948	J70	46	990	L36	35	1032	P3	7	1074	P52	48	1116	Q43	47	1158	R8	3
907	J19	24	949	J71	46	991	L37	38	1033	P4	10	1075	P53	48	1117	Q44	47	1159	R9	3
908	J20	24	950	J72	47	992	L38	39	1034	P5	10	1076	P61	48	1118	Q45	45	1160	R10	3
909	J21	24	951	J73	47	993	L39	44	1035	P6	10	1077	P63	20	1119	Q46	45	1161	R11	3
910	J22	25	952	J74	48	994	L40	47	1036	P7	10	1078	P64	7	1120	Q47	45	1162	R12	3
911	J23	25	953	J75	43	995	L41	45	1037	P8	10	1079	Q1	7	1121	Q48	45	1163	R13	3
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913	J25	28	955	J78	7	997	L43	22	1039	P11	14	1081	Q3	9	1123	Q52	16	1165	R15	3
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917	J28B	30	959	LP1	33	1001	L47	23	1043	P15	16	1085	Q9	29	1127	Q56	9	1169	R19	4
918	J28C	30	960	LP2	33	1002	L48	10	1044	P16	16	1086	Q10	30	1128	Q57	45	1170	R20	4
919	J28D	30	961	LP3	33	1003	L49	3	1045	P17	17	1087	Q11	30	1129	Q59	45	1171	R21	4
920	J29	32	962	LP4	33	1004	L51	18	1046	P18	17	1088	Q12	31	1130	Q60	17	1172	R22	4
921	J30	32	963	LP5	33	1005	L500	49	1047	P20	17	1089	Q13	32	1131	RP17	21	1173	R23	4
922	J31	33	964	LP6	33	1006	L501	51	1048	P22	17	1090	Q14	32	1132	RP18	21	1174	R24	4
923	J32	33	965	LP7	33	1007	L502	7	1049	P24	17	1091	Q15	32	1133	RP20	21	1175	R25	4
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1507	R394	34	1549	R437	38	1591	R491	42	1633	R538	47	1675	R594	9	1717	R1548	51	1759	R1590	6
1508	R395	34	1550	R438	38	1592	R492	42	1634	R540	48	1676	R595	9	1718	R1549	51	1760	R1591	6
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